Fast and Physically-Accurate Estimation of Single Event Transient Pulses From Radiation-Induced Transient Currents Measured in a Single MOSFET: A Simulation-Based Case Study in Bulk CMOS Logic Circuits

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***Abstract*— A fast and physically-accurate estimation technique of single event transient voltage pulses in logic circuits is evaluated in a bulk CMOS technology. The technique handles voltage dependency of radiation-induced transient responses of an irradiated MOSFET without time-consuming mixed-mode simulations. Simulation tests are performed, and results are compared with those in an SOI technology. This case study demonstrates that its applicability to bulk technologies, indicating that importance of handling parasitic capacitance in the irradiated device for increasing estimation accuracy.**

***Index Terms*— Graphical derivation, heavy ions, integrated circuit radiation effects, semiconductor device radiation effects, single event transients (SETs), soft errors.**

I. Introduction

A SINGLE event transient (SET) is a momentary voltage perturbation observed in a circuit when an energetic particle like a heavy ion strikes a semiconductor device, and it becomes a dominant source of soft error as the device feature size decreases and the clock frequency increases [1]–[4]. To reveal physical mechanisms and evaluate device/process-level radiation tolerance, researchers have meticulously measured and simulated radiation-induced (heavy-ion-induced/pulsed-laser-induced) transient currents in a single MOSFET typically with a drain terminal constantly biased at a power supply voltage [5]–[8]: one recent major goal is successfully estimating SET voltage pulses from the obtained transient currents [8].

One standard approach for the estimations is a use of a double-exponential current-source model [9]–[13]. Typically, researchers use a formula expressed as

$$I = I_0 \left(\mathrm{e}^{-t/\tau 1} - \mathrm{e}^{-t/\tau 2} \right), \tag{1}$$

which is fitted to a transient current waveform observed at a constant bias condition via three parameters, I_0, $\tau 1$, and $\tau 2$. This is a simple and powerful approach, enabling us to estimate SET voltage pulses only with a circuit simulator like SPICE. However, voltage-change effects on the transient currents are not properly implemented. Such a voltage-dependency of the transient currents is required for more realistic estimations of SET voltage pulses particularly in modern device technologies [14].

Mixed-mode device simulations, which carry out both device and circuit simulations simultaneously, are effectual approach to deal with such a voltage dependency [14]–[16]. However, they often demand long computational time and large amount of computational resources.

Our proposed technique is one of the candidates to achieve an ideal balance between the estimation-accuracy and computational-costs [17]. It uses radiation-induced transient currents measured in a single MOSFET under various voltage conditions for properly considering the voltage-change effects. The measured transient currents are stored in a look-up table, and SET voltage pulses are estimated within a table-based circuit simulation framework [12], [18]–[21]. No mixed-mode device simulation is carried out in our technique.

The purpose of this paper is discussing its applicability to bulk CMOS logic circuits. We used an SOI MOSFET in the previous simulation studies, finding small discrepancies between estimated pulse waveforms and those obtained with mixed-mode simulations. We have been considering that such discrepancies are due to parasitic capacitance at the drain terminal and expecting to observe larger discrepancies in bulk technologies. The concept of the estimation technique is briefly reviewed in Section II. In Sections III and IV, computer simulation experiments for evaluation and the results are presented and discussed. The conclusion is given in Section V.

II. Brief description of the estimation technique

Fig. 1 summarizes our estimation technique. Fig. 1(a) illustrates a test circuit: an inverter with a load capacitor, C_{L}. We assume that the inverter's input is grounded and a radiation particle strikes the off-state nMOSFET. Note that a radiation-induced transient current, I_{RI}, flowing through the drain terminal of the nMOSFET should be always equal to a recovery current. The recovery current, I_{REC}, is given by $I_{\mathrm{P}} + I_{\mathrm{C}}$, where I_{P} represents a pMOS drain current, and I_{C} a load capacitance discharge current.

This work was supported in part by the Japan Society for the Promotion of Science under Grant-in-Aid for Scientific Research #18560359.

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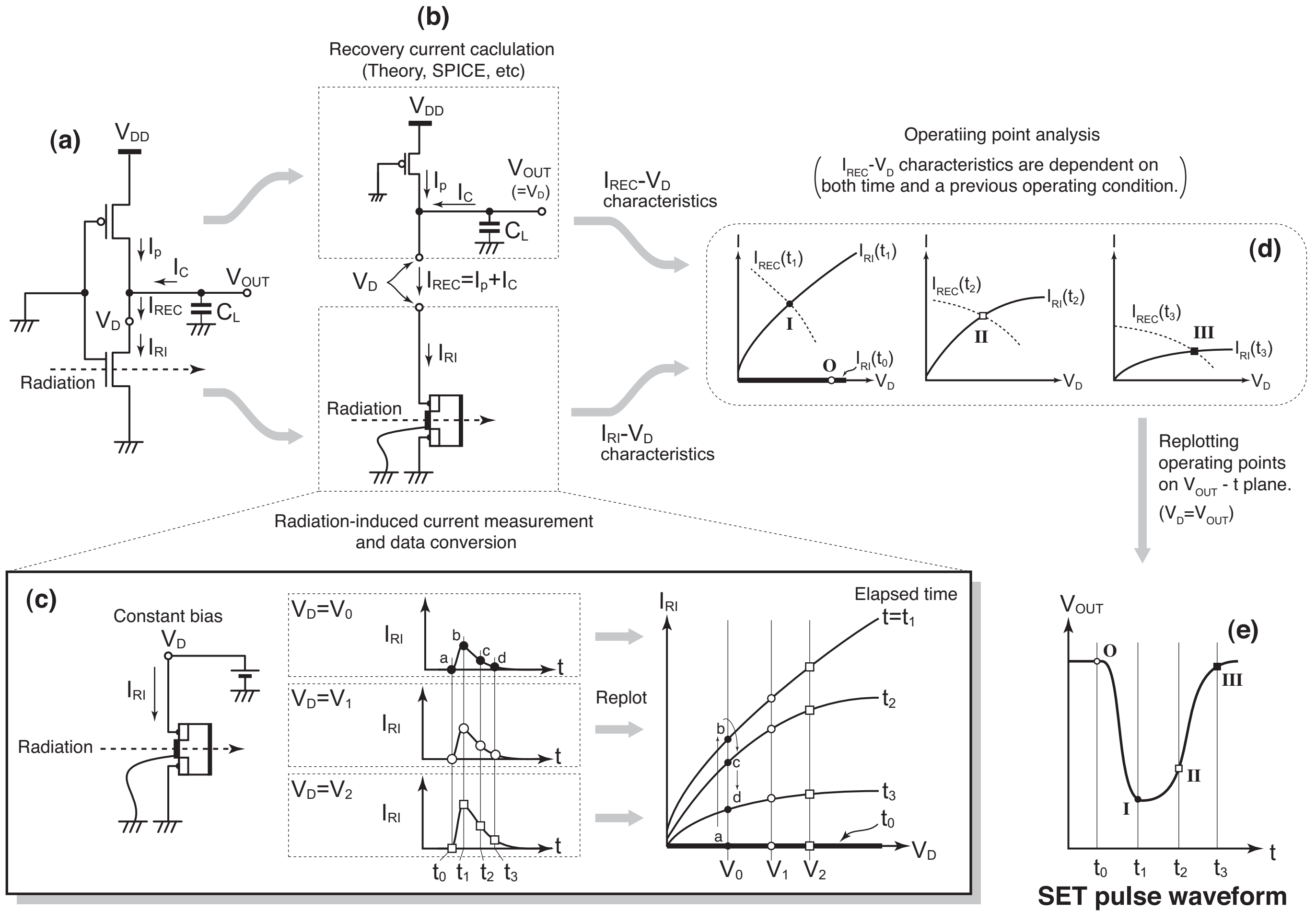


Fig. 1. Basic concept of the SET pulse estimation we proposed in [17]. (a) Test inverter circuit: a recovery current, $I_{\rm REC}$, which is given by adding a pMOSFET drain current, $I_{\rm p}$ and a load capacitance discharge current, $I_{\rm C}$, is always equal to the radiation-induced transient current, $I_{\rm RI}$, flowing through the drain terminal of the nMOSFET. The drain voltage, $V_{\rm D}$, also represents inverter's output voltage, $V_{\rm OUT}$. (b) The inverter is divided into two circuit blocks: the irradiated nMOSFET and the non-irradiated components. (c) Measurement of Radiation-induced transient currents in the single nMOSFET: transient currents are measured as a function of time under various constant $V_{\rm D}$ conditions. The measured currents are replotted as a function of $V_{\rm D}$. (d) Graphical operating point analysis: the inverter's operating point for each time is determined by the intersection of the $I_{\rm REC}$ and $I_{\rm RI}$ curves. (e) SET pulse derivation from the operating points.

As shown in Fig. 1(b), we can divide the inverter into two circuit blocks: the irradiated nMOSFET and the rest of circuit components. In the non-irradiated circuit block, we calculate $I_{\rm REC}$ as a function of the drain voltage, $V_{\rm D}$, with theories, circuit simulations, and so forth. For the irradiated nMOSFET, we prepare $I_{\rm RI}(V_{\rm D})$ curves ($I_{\rm RI}$ vs. $V_{\rm D}$ curves) using the following method illustrated in Fig. 1(c).

We measure $I_{\rm RI}$ as a function of time, t, in the single nMOSFET with a constant $V_{\rm D}$. Changing $V_{\rm D}$, we obtain $I_{\rm RI}(t)$ curves under various $V_{\rm D}$ conditions. We then read out $I_{\rm RI}$ values at an instant of time for each $V_{\rm D}$ and replot them on a $I_{\rm RI} - V_{\rm D}$ plane. We thus obtain $I_{\rm RI}(V_{\rm D})$ curves for each instant of time.

To obtain operating points for the inverter, we plot both $I_{\rm REC} - V_{\rm D}$ and $I_{\rm RI} - V_{\rm D}$ characteristics on a single $I - V_{\rm D}$ plane, as shown in Fig. 1(d). Because $I_{\rm RI}$ should be equal to $I_{\rm REC}$ for each time, the operating point for the inverter at t is given by the intersection of both two characteristics curves at the moment, as illustrated in a conventional graphical derivation method of inverter dc transfer characteristics [22]. Reading out all operating points, we thus obtain an SET voltage pulse waveform, as shown in Fig. 1(e).

In this technique, the $I_{\rm RI}(V_{\rm D})$ curves are stored in a table, and a computer looks up the required data in it. This is categorized as "look-up table (or table look-up) modeling" method, and widely applied in a field difficult to build analytical models. This technique is also used in the previous soft error studies [12], [21], but not used for modeling radiation-induced transient currents.

The $I_{\rm RI}$'s in this technique do not properly include discharging/charging current components due to parasitic capacitors at the drain terminal because each $I_{\rm RI}(t)$ curve is measured at a constant $V_{\rm D}$ condition. This indicates that estimation errors in bulk technologies will become large compared with those in SOI technologies.

III. Simulation Test in a Bulk Technology

To evaluate the applicability of our estimation technique in bulk technologies, we carried out a computer simulation test. We performed 2-D simulations to obtain $I_{\rm RI}(t)$ curves

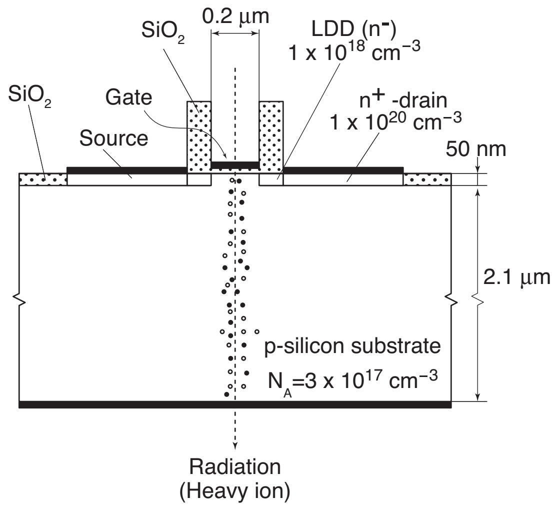


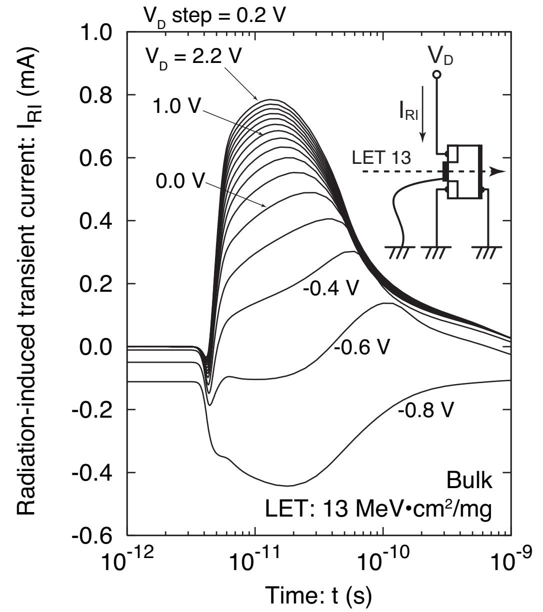
Fig. 2. Diagram of the simulated physical nMOSFET.

for the nMOSFET with the DESSIS device simulator from Synopsys Inc. We then estimated SET pulses in the inverter circuit shown in Fig. 1(a) and compared them with mixed-mode simulation results representing actual pulse waveforms. In this test, we focused only a structural difference in bulk and SOI technologies: only irradiated device structure was changed, and the others, i.e., non-irradiated device models, radiation models, bias conditions, etc., are implemented with the same ones in the previous study.

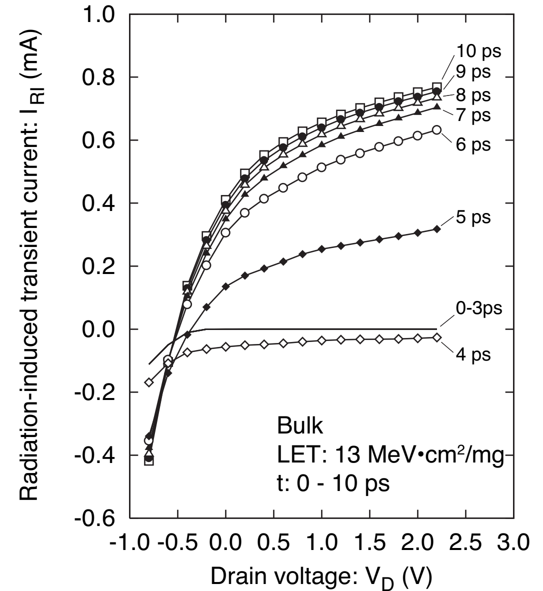
The pMOSFET and the load capacitor C_{L} were implemented with SPICE models in DESSIS. We chose the BSIM3v3.2 SPICE model for the pMOSFET and applied default values to all parameters except for the length, width, and oxide thickness of the gate. The latter three parameters were set at the same values of the physical nMOSFET explained later. We designed the load capacitance C_{L} to be the equivalent of the inverter's input gate capacitance, 2.8 fF, assuming that a copy of the inverter is connected to the output node.

The nMOSFET was implemented with a physical device model. Its dimensions and doping conditions are illustrated in Fig. 2: the gate length was 0.2 μm, the gate oxide thickness was 5 nm, and the virtual gate width was assumed to be 1 μm. This model was created eliminating a 100-nm-thick buried oxide layer in the fully-depleted SOI MOSFET model we used in [7], [17].

A radiation (heavy ion) strike was simulated with the DESSIS HeavyIon module. An electron-hole pair column was created in the device by a carrier-generation function having a Gaussian radial distribution with a $1/\mathrm{e}^2$ characteristic radius of 0.07 μm and a Gaussian time distribution centered on 5 ps with a $1/\mathrm{e}^2$ characteristic time of 0.7 ps. A linear energy transfer (LET) value of the particle was kept constant along the particle track. The track was simulated at a normal incidence at the middle of the gate for the nMOSFET, not the drain area, to keep the same strike position as used in the previous SOI-based study. Note that the power supply voltage, V_{DD}, was kept constant at 2.0 V during the simulations.



(a)



(b)

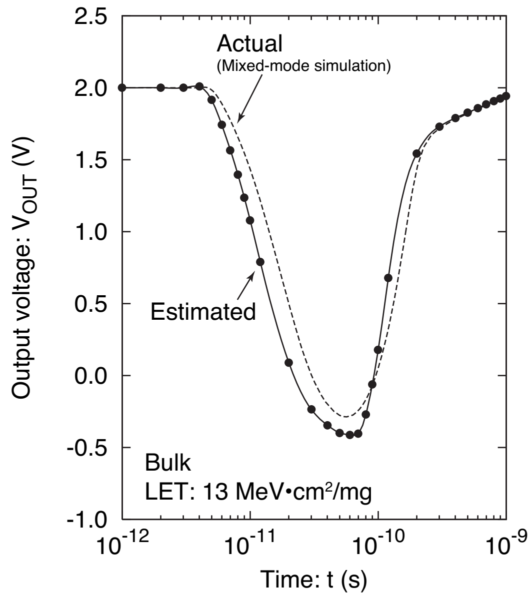
Fig. 3. Simulation results for the single bulk-nMOSFET under 13-MeV·cm^2/mg heavy ion impact. (a) $I_{\mathrm{RI}} - t$ characteristics under various V_{D} conditions. (b) Example of $I_{\mathrm{RI}}(V_{\mathrm{D}})$ curves used in SET pulse estimations.

IV. Results and Discussion

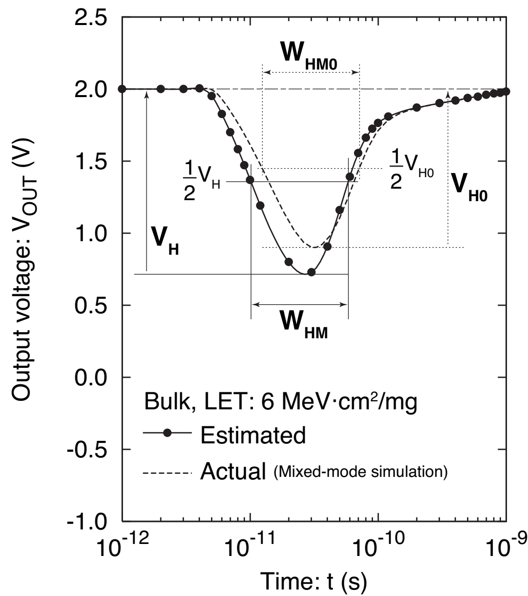
Fig. 3(a) shows simulated $I_{\mathrm{RI}}(t)$ curves for the single bulk-nMOSFET under 13-MeV·cm^2/mg heavy ion impact. From these results, we obtained a set of $I_{\mathrm{RI}}(V_{\mathrm{D}})$ curves, which examples are illustrated in Fig. 3(b).

The estimated SET voltage pulses from the $I_{\mathrm{RI}} - V_{\mathrm{D}}$ characteristics are shown in Fig. 4. These figures show fairly good agreements between the estimation results and the actual waveforms obtained with mixed-mode simulations, thus demonstrating the effectiveness of our estimation technique in bulk technologies.

We compared estimation accuracy in bulk and SOI tech-

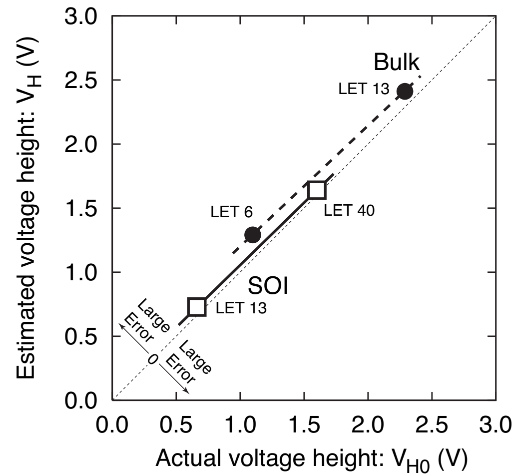


(a)

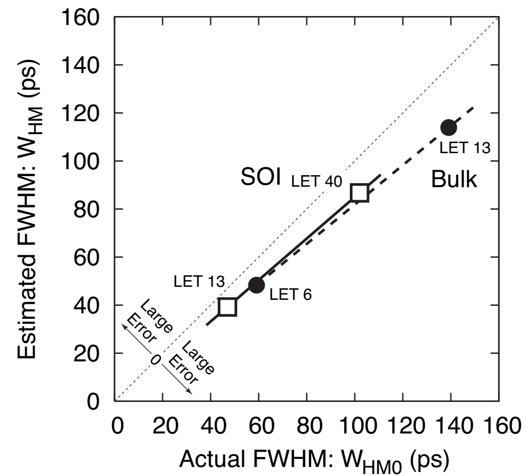


(b)

Fig. 4. SET pulse estimation results: (a) LET $= 13$ MeV$\cdot$cm^2/mg and (b) 6 MeV$\cdot$cm^2/mg. Mixed-mode simulation results are superimposed for references representing the actual SET pulses (dashed line). Extracted parameters explained in the bottom are plotted in Fig. 5.



(a)



(b)

Fig. 5. Relationships between actual pulses and estimated pulses: (a) voltage heights, (b) temporal widths (full-width at half maximum).

nologies. Fig. 5(a) shows the relationship between actual pulse heights, V_{H0}'s, and estimated pulse heights, V_{H}'s, for each technology. Fig. 5(b) shows the relationship between actual pulse widths (FWHM), W_{HM0}'s, and estimated pulse widths, W_{HM}'s. In these figures, we observe that the estimation errors in the bulk technology are larger than those in SOI as we expected. We can conclude that these estimation errors are derived from the parasitic capacitors at the drain terminal in the irradiated nMOSFET. Extracting such parasitic capacitors and properly taking their effects into consideration on the estimation process will improve the accuracy of the estimation.

V. Conclusion

We evaluated our fast and physically-accurate single event transient pulse estimation technique in a bulk CMOS technology. The most essential aspect of the technique is a use of a table storing radiation-induced transient-current data observed under various bias conditions. This enables us to estimate single event transient pulses in logic circuits with properly handling a voltage dependency of the radiation-induced transient currents without time-consuming mixed-mode device simulations.

A simulation test was performed in a bulk technology, and results were compared with those in an SOI technology. This case study demonstrates that its applicability to bulk technologies and indicates that importance of handling parasitic capacitance in the irradiated device for increasing estimation accuracy.

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