

Assessing the Impact of Scaling on the Efficacy of Spatial Redundancy based SER Mitigation Schemes

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Abstract—A novel circuit-level simulation strategy to assess the impact of charge sharing on the upset rate of redundancy based radiation hardened designs is introduced. Accelerated measurements conducted at the Los Alamos National Laboratory show a 10x or better reliability of hardened latches over standard latches for 45nm and 90nm implementations. Despite this encouraging trend, our simulations project that compact redundancy hardened designs will have soft error rates similar to non-hardened designs within a few technology generations if no additional mitigation techniques are applied to reduce the impact of charge sharing.

Index Terms—SER, DICE, SEUT, BISER, SET, charge sharing, MBU, radiation, soft error, redundancy

I. INTRODUCTION

Soft errors (SE) are random errors that are caused by cosmic rays and alpha-particles emitted by radioactive isotopes located within about 50 μ m of the Si surface [1, 2]. For terrestrial applications high-energy neutrons are the dominating source of upsets caused by cosmic radiation. Radiation-induced soft error rates (SER) of modern chips are projected to increase with each technology generation if no additional mitigation techniques are implemented [2, 3]. One such class of mitigation techniques are space redundancy based schemes that at the very least duplicate the number of storage nodes or cells. Examples are DICE [4], SEUT [5, 6, 7], circuit-level TMR [8], and BISER [9]. They all have in common that data can be corrupted by one particle strike if more than one storage node or device collects charge, i.e. when charge sharing occurs.

It is well known that multiple bit upset (MBU) rates in SRAM arrays are increasing exponentially with scaling, indicating that more charge is shared among neighboring

SRAM cells with each generation [3, 15]. In the light of this scaling trend it is not known if and when space redundancy based SER mitigation techniques will cease to be effective. Recently, several groups have started investigating the impact of scaling on MBU using 3D device simulations, or mixed-mode simulations [10, 11]. These simulations can take days to finish simulating the impact of only one particle strike [10].

In the following a novel methodology is described that capable of estimating radiation induced error rates of redundancy based radiation hardened circuits based on fast circuit-level simulations. Our novel simulation strategy is then applied to determine the impact of technology scaling on the upset rates of hardened devices that utilize local redundancy.

II. CHARGE SHARING SIMULATION TECHNIQUE

A. Simulation Strategy

Single bit upset (SBU) rate simulation techniques have been described in detail by Freeman et al. and Walstra et al. [12, 13]. The nominal error rate of a node can be modeled as a function of its critical charge (Q_{crit}) and the charge collection area (A) [13]. The critical charge equals the minimum charge that needs to be collected by a node to corrupt the data stored in the device. The soft error rate essentially reflects the probability that a charge $\geq Q_{crit}$ is collected. Q_{crit} and A reflect the circuit impact on the soft error rate, whereas the process susceptibility to radiation is implicitly accounted for in the parameters of the analytical SER functions. The key advantage of this modeling strategy is that it decouples the process and circuit impact on SER.

To simulate Q_{crit} the charge collection kinetics (i.e., charge collection waveform) need to be known. Device-level simulations are frequently used to derive an “average” or “effective” current waveform [11, 13]. Once the average charge collection waveform $I(t)$ has been determined, Q_{crit} can be estimated using circuit-level simulations for every node and circuit. This is achieved by connecting an independent current source $I(t)$ to the node of interest.

The amount of collected charge - which equals the area under the $I(t)$ vs time (t) curve - is then varied until the minimum charge that upsets the circuit has been found. This is by definition the critical charge Q_{crit} . In our study the output

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nodes of the investigated latches are monitored for errors (q in figure 1). Q_{crit} and A – extracted from physical layout – are then plugged into an analytical SER equation that has been calibrated using measured SBU data collected from dedicated test-chips [13].

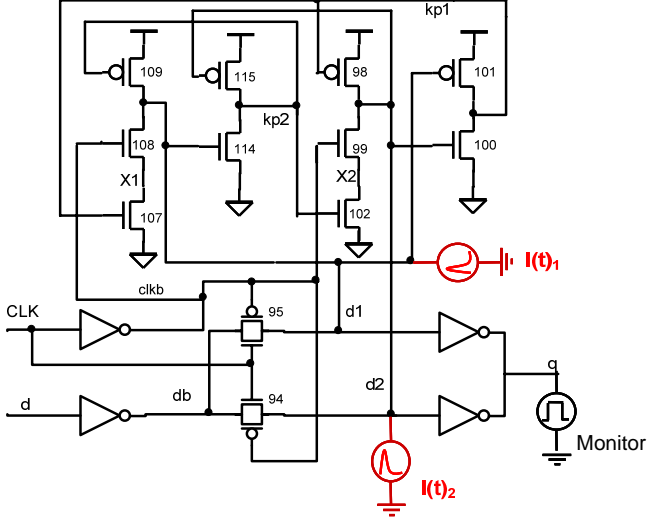


Figure 1: Two current sources $I(t)$ are attached to the nodes of interest (d1 and d2) as shown for an SEUT device. The ratio of injected charges is fixed during each Q_{crit} simulations and equals R (see text).

The proposed novel strategy of estimating the error rates of electrically coupled nodes which collect charge via charge sharing is similar to the SBU methodology just described. Throughout this work electrically coupled nodes are divided up in a primary and a secondary node. Which node is the primary or the secondary is completely arbitrary.

Our strategy requires the knowledge of $P(Q,x,A)$ which denotes the probability of collecting charge Q at the secondary node (with collection area A). The distance between the nodes equals $x \mu\text{m}$. Strategies to derive $P(Q,x,A)$ are discussed briefly in section B.

The impact of charge sharing on the upset rate of redundancy hardened circuits can then be estimated using circuit-level simulation tools which are orders of magnitude faster than physical device simulations. *The strategy is to attach not one waveform (i.e., current source) as described above (SBU), but two waveforms at the primary and secondary nodes* (see figure 1). Both waveforms have identical rise and fall time constants, and the peak currents (I_{peak}) are reached at the same time¹. The waveforms $I_1(t)$ and $I_2(t)$ are inserted at two coupled nodes and the critical charge Q_{crit} of the primary node (that is the very definition of the primary one) is determined for various ratios of collected charges (i.e. I_{peak} values) between both nodes². *The key point in our strategy is that Q_{crit} of the primary node is a function of*

¹ Waveforms for which I_{peak} at a secondary node is reached considerably later than at the primary node reflect charge deposited farther away from the collection area. Such a scenario is most probably characterized by a relatively small amplitude (i.e., I_{peak}) value whose impact on SER, the authors believe, can be neglected.

² This implicitly assumes that a 3 node strike scenario is highly improbable. Our methodology could easily be extended to include this case.

the charge collected at the secondary node (Q_s) which is collected with probability $P(Q_s,x,A)$, where x equals the distance between both nodes. The nominal SER function $SER(Q_{crit}(Q_s), A)$ equals the calibrated SBU one, since charge collected at secondary nodes does not impact the probability of collecting charge at primary nodes. In the presence of charge sharing the average soft error rate $\langle SER(x) \rangle_i^j$ of a circuit comprising of primary node j and secondary node i can then be expressed as

$$\langle SER(x) \rangle_i^j = \frac{\int_0^\infty P(Q_s^i, x, A_i) * SER(Q_{crit}^j(Q_s^i(x), A_j)) dQ_s^i}{\int_0^\infty \int_0^\infty P(Q_s^i, x', A_i) dQ_s^i dx'} \quad (1)$$

Q_{crit}^j of primary node j is a function of the charge collected at secondary node i , if both nodes are electrically coupled. If several diffusions are attached to the primary or secondary node, all SER contributions calculated according to equation (1) need to be added up.

$Q_{crit}^j(Q_s^i(x), A_j)$ is simulated by fixing the ratio R of the current peak values (I_{peak}) of $I(t)_p$ and $I(t)_s$ and varying I_{peak} . Q_s^i then equals $Q_{crit}^j * R$.

Since the assignment of primary and secondary nodes is completely arbitrary, one has to average over both cases, i.e., each node is once a primary and once a secondary node.

B. Charge Collection Probability $P(Q,x,A)$

Neutrons generate charge indirectly via nuclear reactions with Si and other materials present in a modern chip. Those nuclear reactions result in the emission of secondary particles that generate electron/hole pairs in Si [1, 14]. A wide range of energies and type of emitted ions exist, all with their distinct probabilities. Charge is then collected by reverse biased junctions. For advanced technologies those energetic particles may traverse the sensitive volumes of several nodes resulting in more than one node collecting charge. One strategy to determine $P(Q,x,A)$ is to run exhaustive 3D device simulations. Another option is to use directly measured MBU data of for instance SRAM arrays and to extract the probability distribution as a function of location as described in detail in reference 3. This is the method of choice in this work.

Once $P(Q,x,A)$ has been determined, circuit-level simulations can be used to estimate the error rates of redundancy hardened circuits, as was discussed in section A.

It is assumed that to first order $P(Q,x,A)$ does not depend on circuit topology. Therefore, if $P(Q,x,A)$ has been extracted from measured MBU SRAM data, it can be applied to different cells and is assumed to describe the charge collection in all charge sharing situations. The size dependence (x) of $P(Q,x,A)$ is derived from MBU cluster statistics of different sizes, whereas the collected charge dependence is derived from MBU data of a fixed size collected at different voltages (critical charges). Selected results extracted from 45nm MBU data are shown in figure 2.

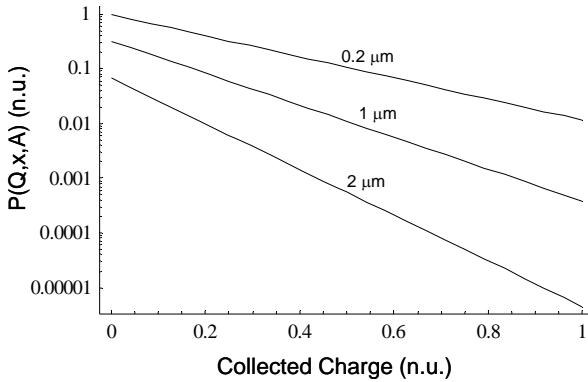


Figure 2: Charge collection probability distribution function $P(Q,x,A)$ plotted as a function of collected charge Q and distance extracted from 45nm MBU data. The cluster-size (x) and collected charge (Q) dependence has been fitted to experimental data using exponential functions.

The collected charge Q reflects the integrated charge under the current waveform $I(t)$ which describes the radiation-induced charge collection kinetics. *It is important to realize that $P(Q,x,A)$ and the distribution of charge collection time constants completely describe the charge sharing/collection phenomenon.* The time constants of $I(t)$ are known to depend on the strike and circuit geometries [11] and one expects that a whole range of time constants need to be accounted for in error rate projections. However, SBU studies have shown that using one single average waveform (i.e., one set of rise and fall time constants) yields sufficiently accurate results [13].

III. EXPERIMENTAL SETUP

Neutron-induced error rates of SEUT devices have been measured at the Los Alamos Laboratory Weapons Neutrons Research (WNR) facility, New Mexico. These radiation experiments comply with the JEDEC JESD89 testing standard [16].

The SEUT test-chips were implemented in a 45nm high-k metal gate process. 90nm SEUT data have been collected by a different team during a previous Los Alamos trip [5-7].

Each 45nm test-chip contains several thousand SEUT devices and each board has a capacity of 22 test-chips that are arranged in a circle whose diameter is smaller than the LANL neutron beam diameter. Several boards can be daisy chained together to increase the number of detectable errors.

The SEUT test-chips communicate to the host PC through the parallel port. Data are shifted in using 2 non-overlapping clocks. After all data have been written, clocks are stopped and the parts are exposed to the neutron beam at normal incidence. After a predefined exposure time at a predefined voltage, the neutron beam is turned off, the clocks restarted and the latch data are shifted out. Due to low upset rates of the studied 45nm SEUT devices, upset rates at only one voltage (0.7V) and one data pattern only (checkerboard) was investigated.

IV. INVESTIGATED DESIGNS

The SEUT design strategy and architecture is described in detail in references 5-7. Figure 1 shows a schematic of a hardened latch implemented in a 45nm CMOS process.

Design details of BISER can be found in reference 9.

V. RESULTS AND DISCUSSION

Based on the experimental results presented in figure 3, one might conclude that redundancy hardened latches show technology independent upset rates. In the following discussion, however, we will learn that this conclusion is most probably incorrect and that process scaling might render latches that employ local redundancy hardening schemes ineffective within a few technology generations.

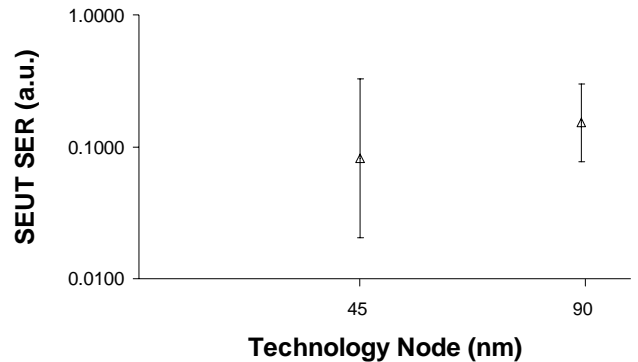


Figure 3: Measured SEUT SER rates at 0.7V (45nm) and 0.8V (90nm) including estimated upper and lower 90% confidence intervals. Results are specified relative to the 45nm reference latch SER.

In the following results of charge sharing simulations of SEUT devices (90nm and 45nm) and 45nm BISER devices will be discussed.

A. SEUT

Figure 4 illustrates the dependence of Q_{crit} of primary node d1 (figure 1) on the amount of charge Q_s collected at secondary node d2. Two distinct regions can be observed. At low Q_s values Q_{crit} initially decreases steeply with increasing Q_s . The studied device could not be upset for Q_s values below ~ 0.55 . Therefore a Q_s threshold exists below which the primary node cannot be upset, independent of how much charge is collected. In other words, a minimum amount of charge needs to be collected at the electrically coupled secondary node, or the device cannot be upset via charge sharing. The exact threshold depends on various parameters, such as supply voltage, technology and circuit type. In region II, Q_{crit} shows a weaker dependence on Q_s . The fact that both nodes are coupled is reflected by the decreasing critical charge of the primary node with increasing charge collected at the secondary node.

Since the probability $P(Q_s, x, A)$ of collecting charge Q_s at the secondary node decreases exponentially with increasing Q_s and the soft error rate increases with decreasing critical charge Q_{crit} of the primary node, only a small window of collected charges Q_s exists that yields a significant soft error rate

contribution (P^*SER in figure 4). The observed dependence of Q_{crit} and P^*S on Q_s is not limited to the investigated SEUT device, but characteristic of all redundancy hardened devices with coupled nodes (i.e., nodes with feedback). However, devices with little or no feedback (TMR and BISR for instance) show a slightly different dependence and will be discussed below. Nevertheless, equation (1) provides an accurate description of all discussed devices.

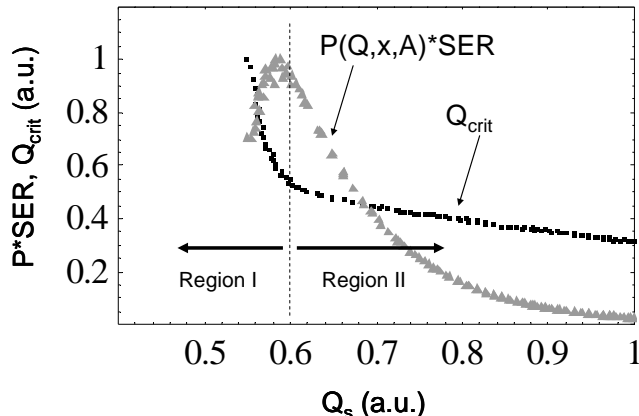


Figure 4: Q_{crit} of d1 and P^*SER values plotted as a function of charge Q_s collected at coupled node d2 of the SEUT device shown in figure 1.

For the 45nm SEUT device we simulated the neutron-induced error rates for various coupled node distances and supply voltages to investigate the robustness of the full design space. We also simulated SBU rates of clock node hits.

Increasing diffusion distances x , assuming the overall node capacitances remain the same, results in a decrease in P^*S and consequently the SER contribution due to charge sharing. The main reason lies in a lower probability to collect a sufficient amount of charge Q_s at larger distances.

Increasing the power supply voltage at constant distance x shifts P^*S towards larger collected charges at the coupled node and also reduces the charge-sharing induced SER of the device substantially due to the fact that $P(Q_s, x, A)$ decreases exponentially with increasing Q_s .

Table 1: Simulated versus measured SEUT SER rates. Results normalized to reference non-hardened 45nm design.

Device	Technology (nm)	Vcc (V)	Nodes	min Distance (n.u.)	SER (n.u.)
SEUT-meas	45	0.7	NA	1	0.0818
SEUT-meas	90	0.8	NA	5	0.1518
SEUT	45	0.7	1->0 only	1	0.0257
SEUT	45	0.7	0->1 only	2.5	0.0007
SEUT	45	0.7	all	1	0.0132
SEUT	45	0.7	clkb	NA	0.1051
SEUT	90	0.8	all	5	3.97E-08
SEUT	90	0.7	all	1	0.0350
SEUT	90	0.8	clk node	NA	0.0934

Table 1 summarizes simulated and measured (first 2 rows) SEUT results. “all” in the Nodes column denotes that SER contributions of all N-N and P-P coupled node combinations have been accounted for. This does not include upsets where both NMOS and PMOS devices collect charge simultaneously. It is believed that N-P upsets are very improbable because the collected charges have to overcome

the Nwell barrier [10]. Node distances in table 1 equal the minimum node distance between coupled node pairs relative to the minimum 45nm one. Clearly, the d1/d2 node pair is the largest contributor to the SEUT neutron-induced error rate due to charge sharing, mainly because of the relatively small separation between two d1 and d2 NMOS diffusions. This asymmetry is not observed in our experimental 45nm SER data, which provides further evidence that the measured upset rates are not the result of charge sharing.

Clock node SBU SER simulations have been conducted according to the methodology described in references 13 and 17. Hits on this clock node temporarily open the downstream transmission gate which potentially corrupts data stored in the latch (radiation-induced race [17]). Results fall within the 90% confidence intervals of the measured 45nm and 90nm SER values. Further, our clock node simulations project roughly equal 1->0 and 0->1 upset rates, which is consistent with our experimental observations. Please note that in a realistic circuit environment (FF or latch along a data path for instance), clock node upsets contribute to the sequential SER [17].

The measured SEUT SER results have fairly large error bars due to the small number of detected errors. It is therefore not possible to extract the SER contribution due to charge sharing from the measured upset rates. The only statement that can be made is that contributions due to charge sharing must be smaller than failure rates due to clock node strikes. This is an admittedly weak statement but consistent with the simulation results. In the remainder of the discussion section we assume that the introduced simulation strategy for estimating the impact of charge sharing is accurate.

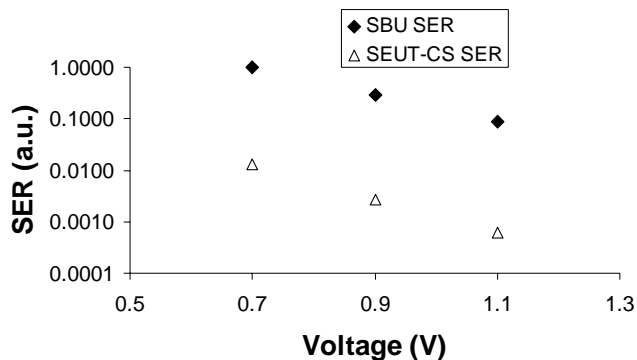


Figure 5: Simulated voltage dependence of single-bit upset rates of the reference 45nm latch (SBU) and 45nm SEUT upset rates due to charge sharing.

The voltage dependence of single bit upset failure rates (SBU) and upset rates of SEUT devices due to charge sharing (CS-SER) are plotted in figure 5. Lowering the supply voltage reduces the critical charge for upsetting device nodes which in turn increases the device upset rate. In the case of charge sharing and two or more coupled nodes, lowering the voltage results in reducing the critical charge of the primary node and reducing the charge needed to be collected on the secondary node to upset the device. This explains the somewhat steeper

dependence of the simulated upset rates of SEUT devices relative to the non-hardened reference latch (figure 5).

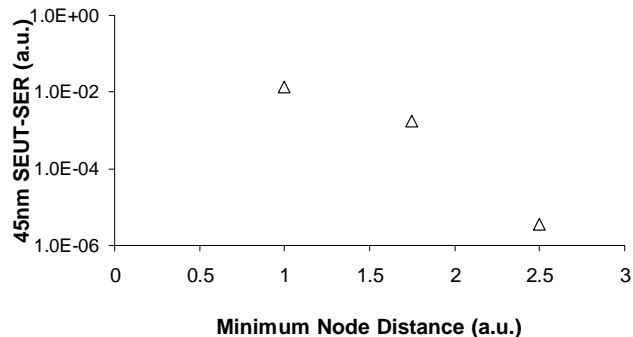


Figure 6: Simulated 45nm SEUT SER vs minimum node separation.

The SER dependence on node separation is an exponential one (figure 6). This is not surprising since MBU SRAM data also show an exponential dependence in cell separation. Doubling the distance yields a $\sim 10x$ decrease in SER for SEUT type devices. Charge sharing is projected to be negligible for the investigated 90nm SEUT device (see simulated values listed in table 1). However, experimental soft error rates are comparable in magnitude to those of the 45nm version (first two rows in table 1 and figure 3), despite the fact that the 45nm device had a $\sim 5x$ smaller minimum node distance. Our investigations indicate that similar to the 45nm implementation, the observed 90nm error rates are dominated by upsets of one of the local clock nodes.

B. BISER

No experimental data are available for this device type and we completely rely on simulations in this case. BISER (or for instance device-level TMR) type designs are similar to SEUT and DICE designs in that several nodes or devices need to be upset to corrupt the data stored in the devices. They differ, however, in that the redundant nodes or devices are not directly coupled through connected transistor channels (i.e., no strong feedback exists). If more charge is collected at the primary or secondary node in the case of SEUT or DICE, then less charge is needed on the other node to upset the device. BISER, however, behaves more like two independent cells. Both need to be upset in order to upset the BISER device itself, but collecting more charge in the scan latch for instance will hardly help with upsetting the non-scan latch.

Q_{crit} of the primary node is almost flat as a function of Q_s until a certain threshold is reached (figure 7). Both latches need to be upset to induce a detectable error. The loads on the both latches are not perfectly balanced, which is why the Q_s threshold is different in value from Q_{crit} in the example shown in figure 7.

Simulated 45nm BISER SER results (table 2) are compared to corresponding SEUT results in table 1. It is important to emphasize that BISER type devices are in general less susceptible to upsets due to higher critical charges than corresponding SEUT devices (i.e. dual interlocked designs). One reason lies in the weaker coupling of state nodes in the

BISER redundant latches. The feedback in the SEUT type devices reduces Q_{crit} and therefore yields higher upset rates even if node distances were the same (see table 2; 2nd row).

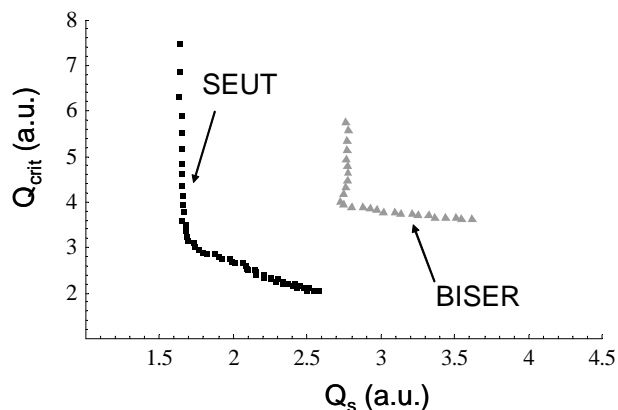


Figure 7: Q_{crit} plotted as a function of Q_s for investigated SEUT and BISER devices. The rectangular shaped Q_{crit} dependence indicates that BISER state nodes are coupled to a lesser degree than SEUT state nodes.

Furthermore, the inherent system/scan topology of BISER leads to spatially distributed storage nodes. As a result, BISER design makes it easier for designers to separate critical nodes farther apart from each other than corresponding nodes in the more compact SEUT type designs. The flipside of the larger separations is a potentially larger cell size. All-in all we believe that comparable BISER based designs (power, area and performance targets) are more robust than corresponding SEUT based designs.

Table 2: BISER charge sharing simulation results. Units are the same as in table 1.

Device	Technology (nm)	Vcc (V)	Nodes	min Distance (n.u.)	SER (n.u.)
BISER	45	0.7	all	3	1.17E-08
BISER	45	0.7	all	1	1.17E-05

C. Technology Trend

Results shown in figures 5 and 6 underline the extreme sensitivity of error rates of device-level redundancy based designs to distance and supply voltage. We have estimated the upset rates of SEUT devices for several process generations at the corresponding typical use conditions (figure 8). 32nm and 65nm results are estimated by scaling critical and collected charges according to expected voltage, distance and capacitance trends. The horizontal arrow in figure 8 denotes error rates of un-hardened latches assuming a flat scaling trend for SBU [3]. Our current projections indicate a crossing at the 22nm node if the SEUT layout is not optimized relative to our 45nm test-chip implementation. The charge sharing induced SER trend (assuming no intelligent layout optimizations) clearly illustrates the risk of diminishing returns of redundancy based hardened cells for future technologies. The steep increase is driven by the decrease in node separations and voltage scaling. Eventually redundancy hardened latches are projected to show upset rates similar to those of non-hardened latches. This trend underlines the need

for additional mitigation techniques that reduce the amount of charge collected at coupled nodes.

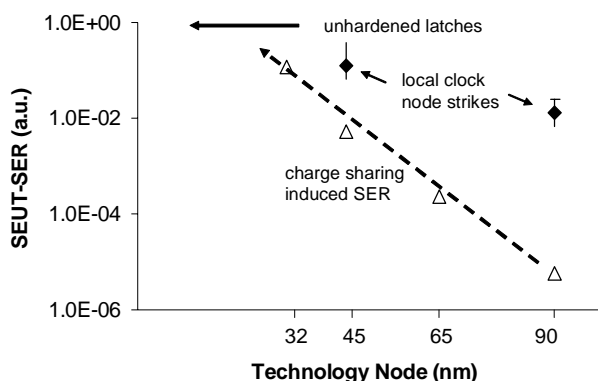


Figure 8: Estimated worst-case technology trend of normalized soft error rates of SEUT/DICE devices at the corresponding nominal use conditions.

At this point not sufficient experimental data are available to rigorously test all aspects of our novel SER simulation methodology. New test-chips are currently being designed that will implement hardened cells with various layout options to better test and calibrate the impact of charge sharing on redundancy hardened devices.

VI. CONCLUSIONS

A novel circuit-level simulation strategy to assess the impact of charge sharing on the upset rate of redundancy based radiation hardened designs is introduced. Simulation results are compared with experimental neutron SER data for 45nm and 90nm SEUT devices. Both SEUT implementations are dominated by clock node strikes rather than charge sharing effects under the investigated experimental testing conditions. Our results are consistent with the limited amount of experimental data available in that they predict a SER contribution due to charge sharing that is well below the clock node strike upset rate for the tested implementations.

BISER type devices have intrinsically lower upset rates due to charge sharing than interlocked designs such as DICE or SEUT. However, in both cases voltage scaling and node separation scaling are projected to render redundancy based hardening designs ineffective in only a few process generations if no additional mitigation techniques are applied.

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