Neutron-Induced Multi-cell and Logic Soft Errors in DRAM Technology and Their Impact on Reliable Server Memory

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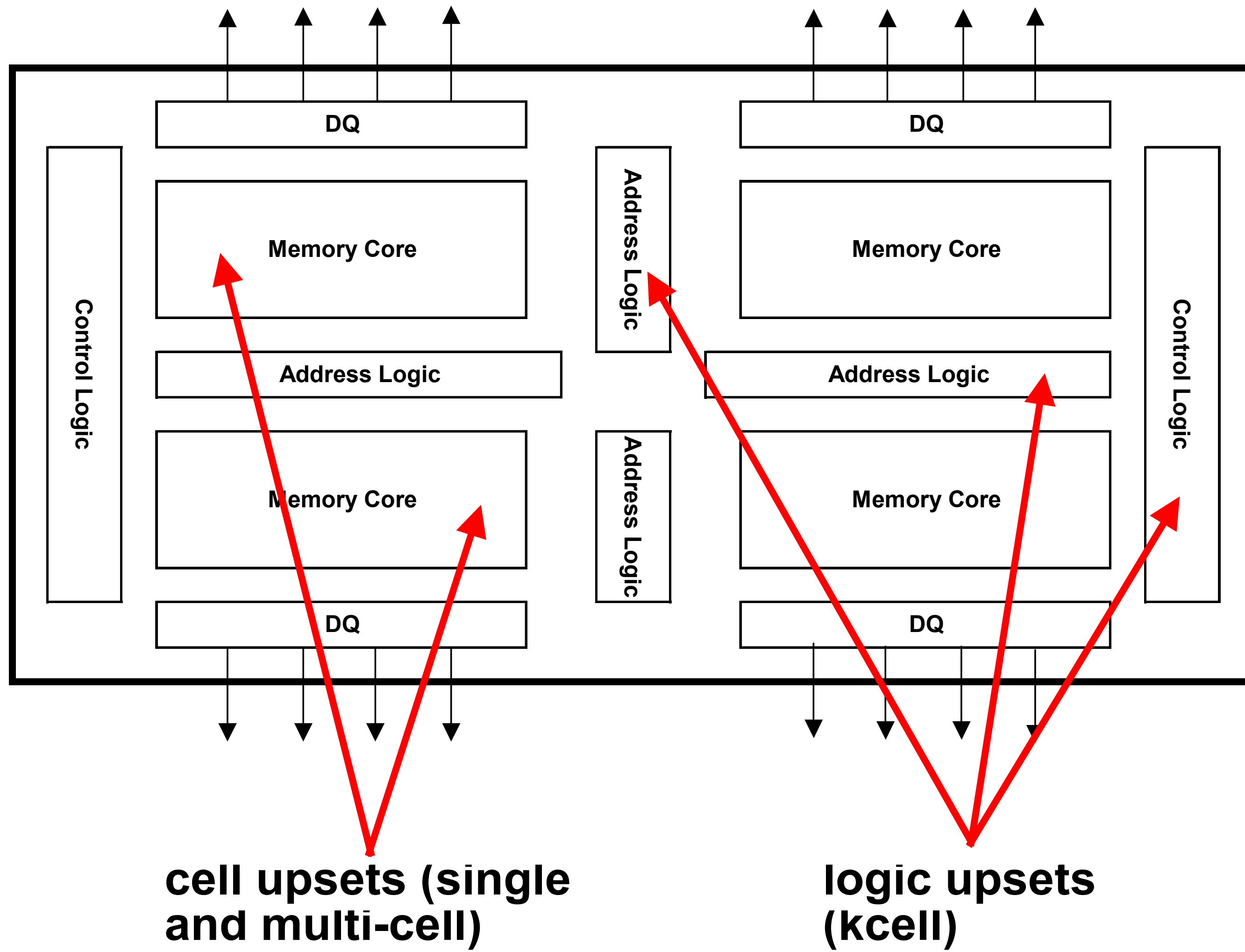
Outline

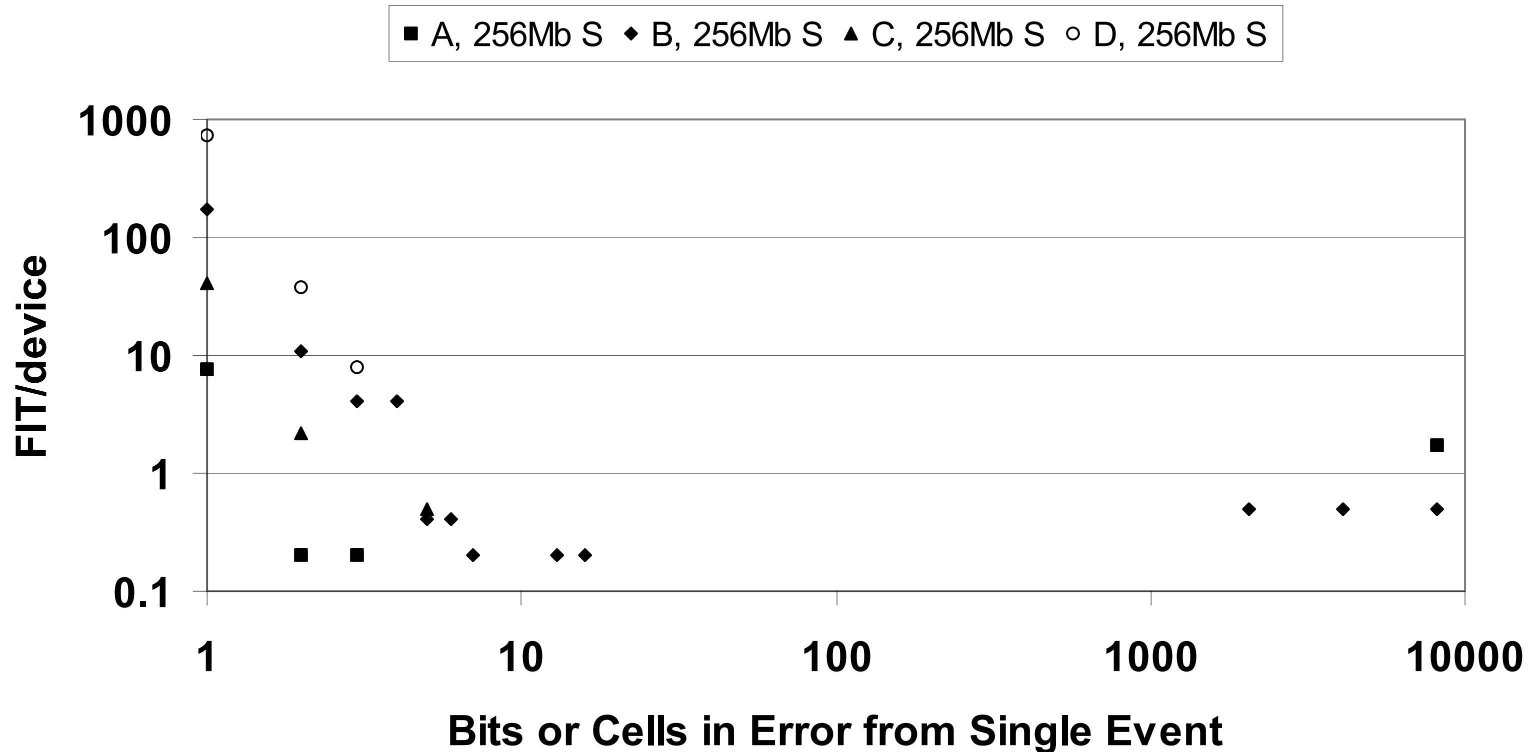
- Soft errors measured in DRAM by accelerated neutron beam at Los Alamos Neutron Science Center (LANSCE)
  - 180nm → 90nm process node
  - Three generations of DRAM design - SDRAM, DDR1 SDRAM, DDR2 SDRAM from six vendors
  - Single cell, multi-cell and logic upsets (kilo-cell) observed
  - Characterization of multi-cell and kcell events
- Impact of soft errors on Error Correction Code (ECC)
- Need for Dynamic Memory Reconfiguration (DMR)
- Future Issues – Fully Buffered Dual Inline Memory Module (FB DIMM)

SER Trends vs Design Rule

Neutron Strikes on DRAM

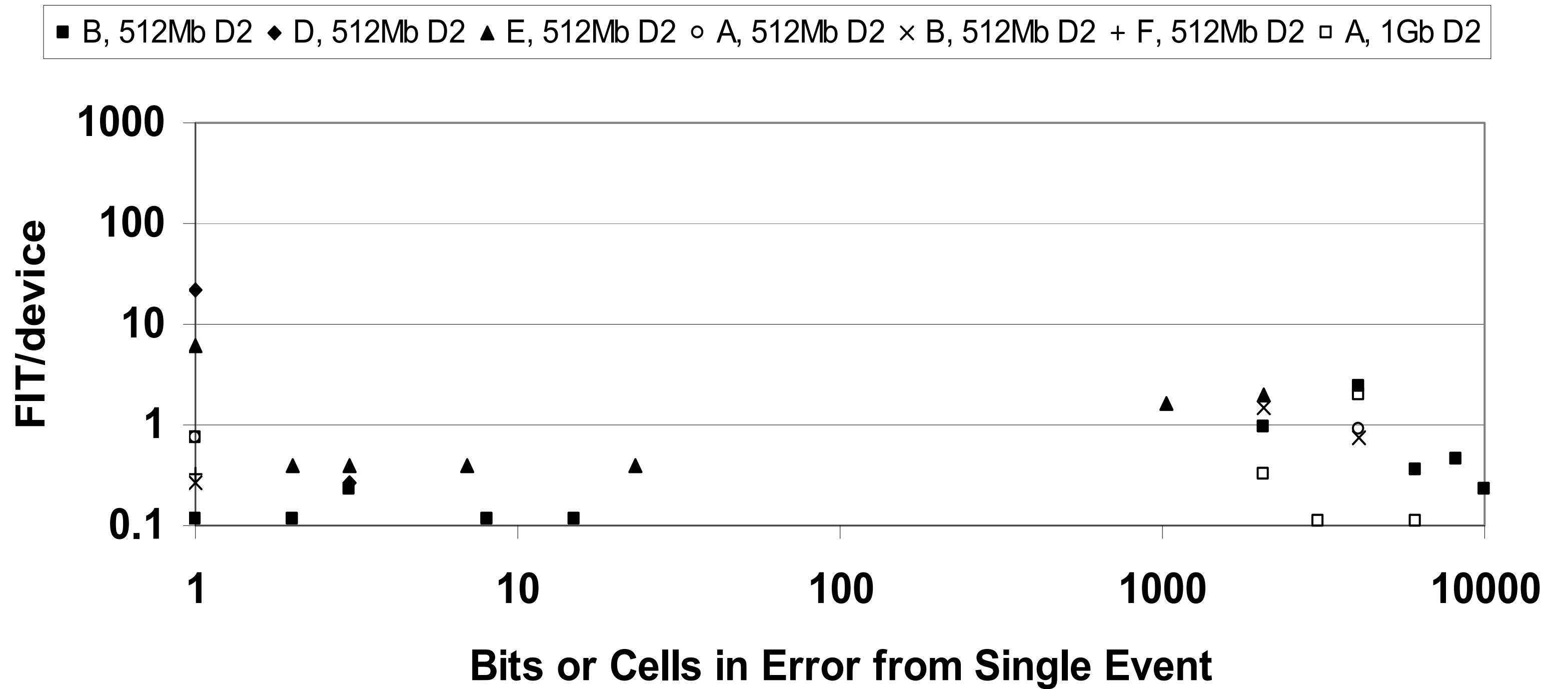


170/180nm DRAM Soft Errors



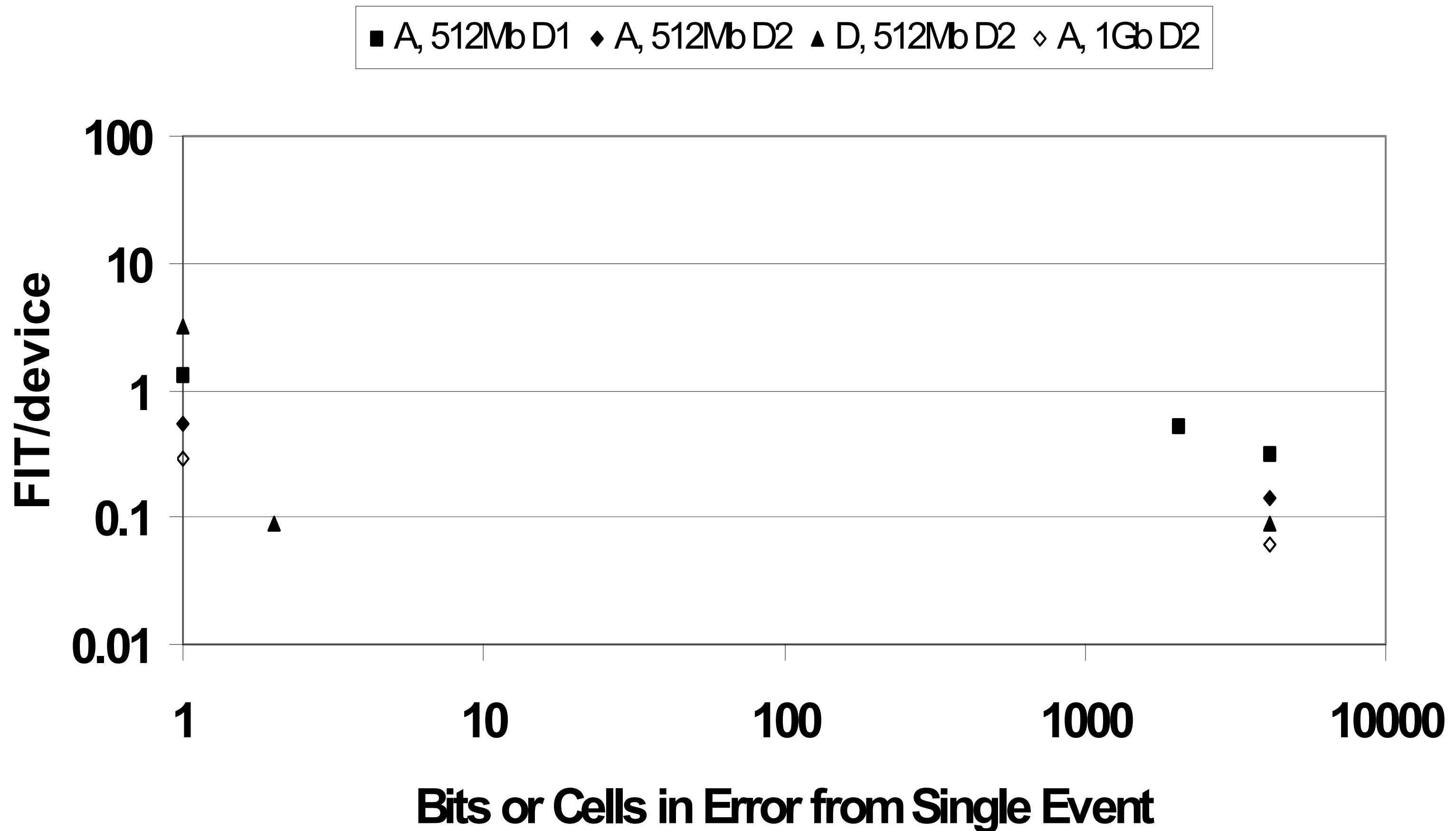
- Rapid multi-cell roll-off – 3 decades in FIT from single cell to 10 cell upset
- Legend: A,B,C,D… = vendor, Density, S = SDRAM, D1 = DDR1, D2 = DDR2

110nm DRAM Soft Errors

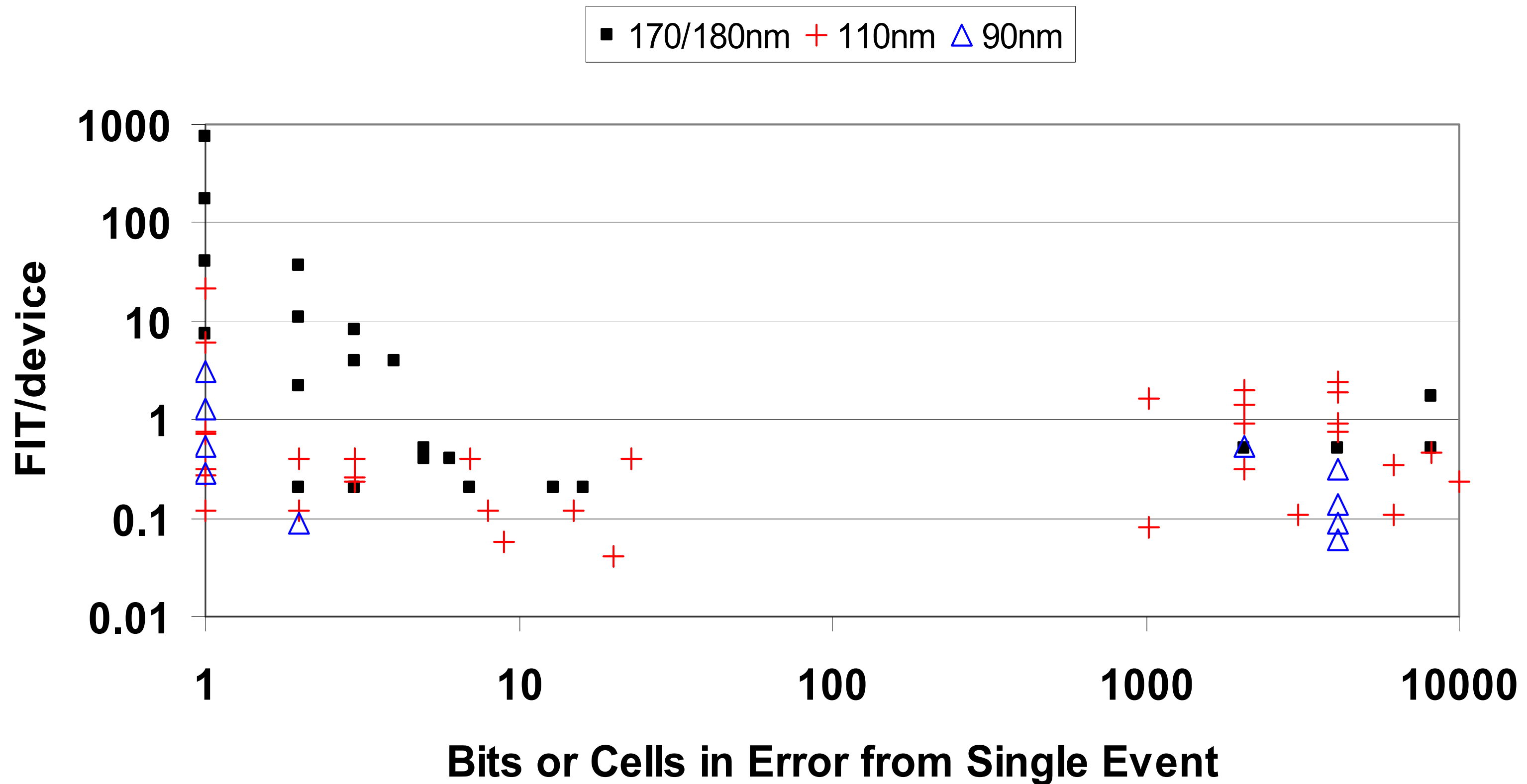


- Multi-cell roll-off less rapid
- Logic (kcell) upsets roughly the same

90nm DRAM Soft Errors

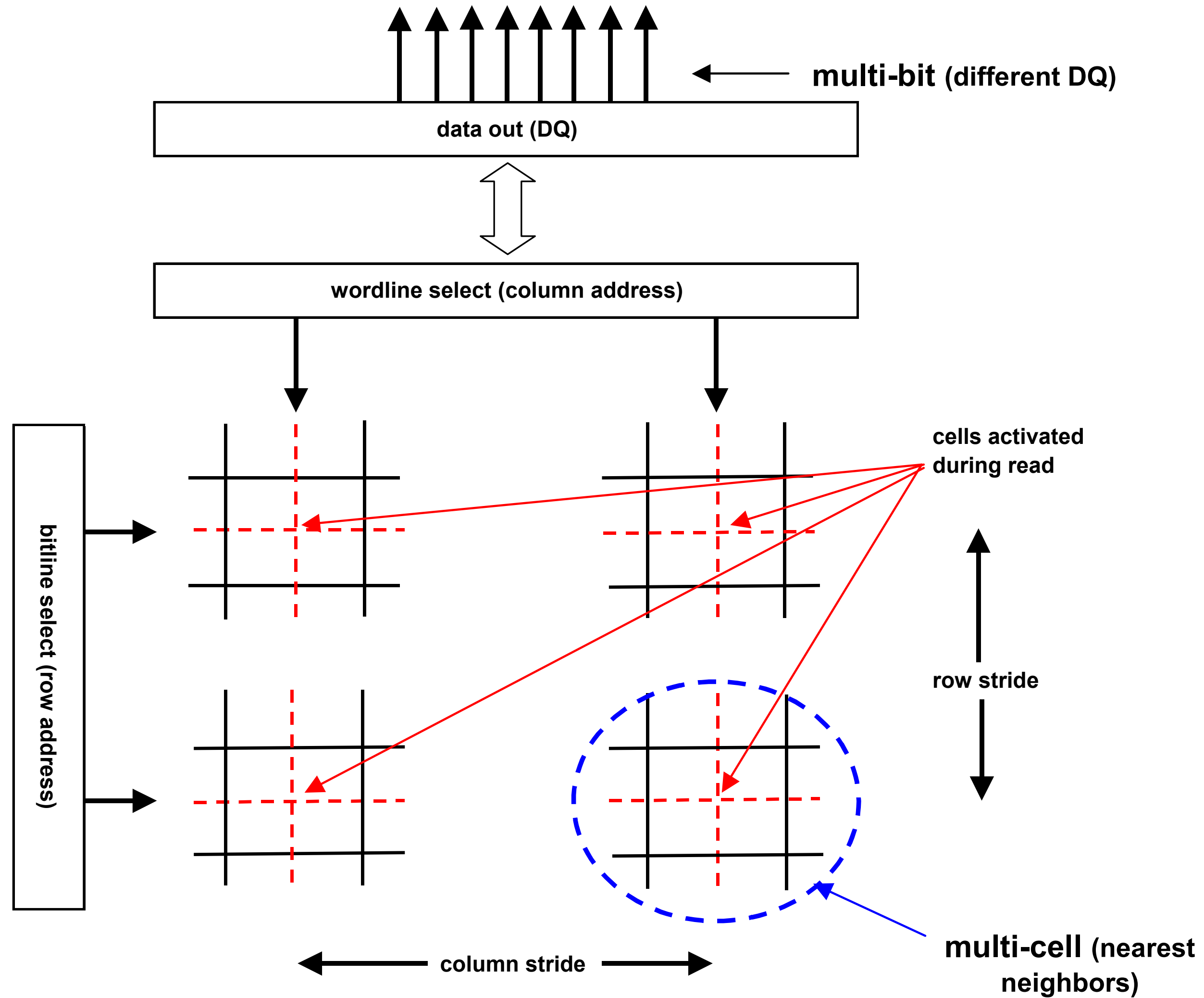


180nm → 90nm DRAM Soft Errors



- Single and multi-cell upset trending downward
- No clear logic upset trend

Array (Physical) Interleave



256Mb 170/180nm SDRAM Multi-cell Events

Ven	2 cell	3 cell	4 cell	5 cell	6 cell	7 cell	13 cell	16 cell	2K cell	4K cell	8K cell
A	3	1									18
B	60	19	5	2	2	1	1	1	3	3	3
C	3			1							
D	97	16	2		1	1					
Sub	163	36	7	3	3	2	1	1	3	3	21
	216								27		
Total	243										

256Mb SDRAM Double Cell Events

Address of Failed Cells			Vendor				TOTAL	Multi-bit?
X=Row	Y=Col.	DQ=I/O	A	B	C	D		
2 adj.	2 adj.	2				6	6	No
2	2	2	1	1		2	4	No
1	2 adj.	2			1		1	No
1	2	2		1		1	2	No
2 adj.	2	1		9			9	No
2	2	1		1			1	No
2 adj.	1	2		23		21	44	No
2	1	2		11		12	23	No
2 adj.	1	1		10	1	46	57	No
2	1	1	1	2	1	9	13	No
1	2 adj.	1		1			1	No
1	2	1		1			1	No
1	1	2	1				1	Yes
TOTAL			3	60	3	97	163	

- Only 1% (1/163) of double-cell events lead to double-bit error
- Note: Address adjacency is logical and not necessarily physical

256Mb SDRAM Triple Cell Events

Address of Failed Cells			Vendor			TOTAL	Multi-bit?
X=Row	Y=Col	DQ=I/O	A	B	D		
3	1	3		2	1	3	No
3	2	2		3	3	6	No
3	1	2	1	3	3	7	No
3	1	1		1		1	No
2	2	2		1	1	2	No
2	1	2		7	8	15	Yes
2	2	1		2		2	No
TOTAL			1	19	16	36	

42% (15/36) events result in multi-bit error

256Mb SDRAM >3 Cell Events

4 CELL UPSET

Event	X-addr	Y-addr	DQ
1	16e6	31d	4
	16e7	31d	14
	16e8	31d	16
	16e9	31d	4
2	1d6e	289	14
	1d6f	289	16
	1d6e	28b	16
	1d6f	28b	16
3	548	16b	13
	549	**16b**	**1+3+14**
4	1fa1	313	9
	1fa4	**313**	**9+11**
	1fa5	313	11
5	94a	78	14
	94b	78	16
	94a	7a	16
	94b	7a	14
6	638	2f4	4
	639	**2f4**	**2+4**
	638	2f5	2
7	**af8**	**258**	**6+8**
	af9	**258**	**6+8**

5 CELL UPSET

Event	X-addr	Y-addr	DQ
1	**95a**	**274**	**2+4**
	95b	**274**	**2+4+14**
2	370	7b	7
	370	**7d**	**5+7+11**
	371	7d	7
3	2f8	112	3
	2f9	112	3
	2fd	112	3
	2fa	311	4
	300	311	4

6 CELL UPSET

Event	X-addr	Y-addr	DQ
1	**1fbc**	**371**	**1+3**
	1fbd	371	1
	1fc0	**371**	**1+3**
	1fc1	371	1
2	**1dc9**	**35**	**5+9+11**
	1dc8	37	11
	1dc9	**37**	**9+11**
3	e3c	22c	2
	e2d	22d	2
	e2e	**22d**	**1+4**
	e2f	**22d**	**1+4**

7 CELL UPSET

Event	X-addr	Y-addr	DQ
1	**928**	**222**	**2+4**
	929	**222**	**2+4**
	926	**223**	**1+4**
	927	223	1
2	cd4	57	10
	cd5	57	8
	cd6	57	12
	cd7	**57**	**6+12**
	cd8	57	10
	cd9	57	10

13 CELL UPSET

Event	X-addr	Y-addr	DQ
1	1adc	20	15
	1ade	20	13
	1adf	20	13
	1ae1	20	15
	1ae3	20	13
	1ae0	22	15
	1ae2	22	13
	1ae3	22	13
	1ae4	**22**	**1+15**
	1ae5	22	15
	1ae6	22	3
	1ae8	22	1

16 CELL UPSET

Event	X-addr	Y-addr	DQ
1	855	3f2	1
	856	3f2	3
	857	**3f2**	**3+13**
	850	3f4	15
	851	**3f4**	**1+15**
	852	**3f4**	**3+13**
	853	**3f4**	**3+13**
	854	**3f4**	**1+15**
	855	3f4	1
	856	3f4	3
	850	3f6	15

76% (13/17) of the events result in multi-bit error

DRAM kcell Events

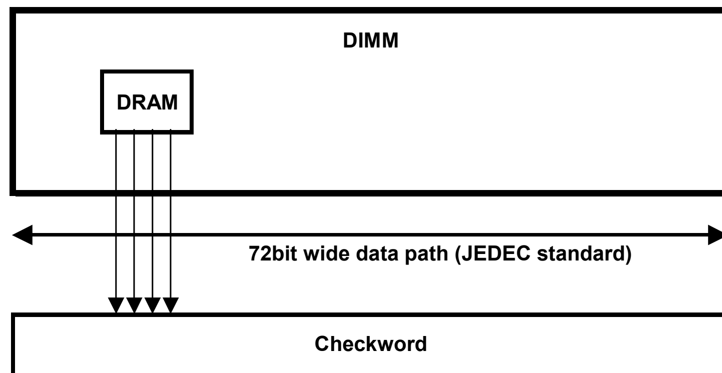
No. of Lines Affected	No. of I/O Affected	Freq. Of Occurrence	Worst Case Error
1 Bitline	4	1%	quadruple-bit
	2	2%	double-bit
	1	4%	single-bit
	all	75%	all bits
2 bitlines		6%	
4 bitlines		6%	
1 wordline		1%	
4 wordlines		5%	

- 96% of logic upsets result in a multi-bit error
- Total of 84 kcell events (27 from 170/180nm and 57 from 110nm and 90nm)
- 5% were NOT clearable by simple rewrite – DRAM reset or power cycle required to clear error

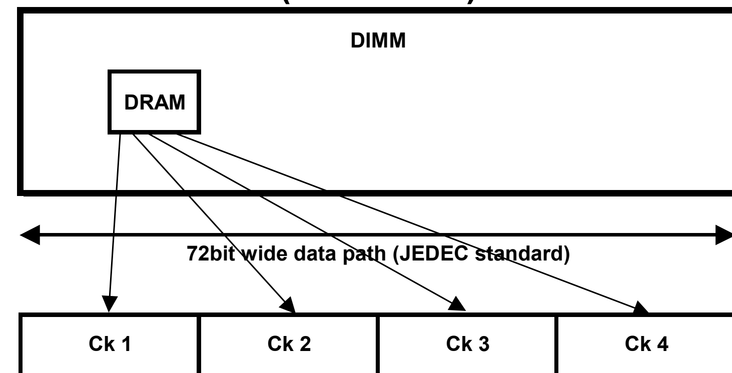
Examples of ECC Implementation

Data bits	ECC bits	Checkword length	Protection
64	8	72	single bit error correct - double bit error detect (SEC-DED)
128	9	137	SEC-DED + 7 spare bits
128	16	144	single Byte correct - double Byte detect (SBC-DBD with B=4bits)

DRAM DQ ----> single checkword



DRAM DQ ----> multiple checkwords (interleave)



Soft Error Behavior of ECC Codes

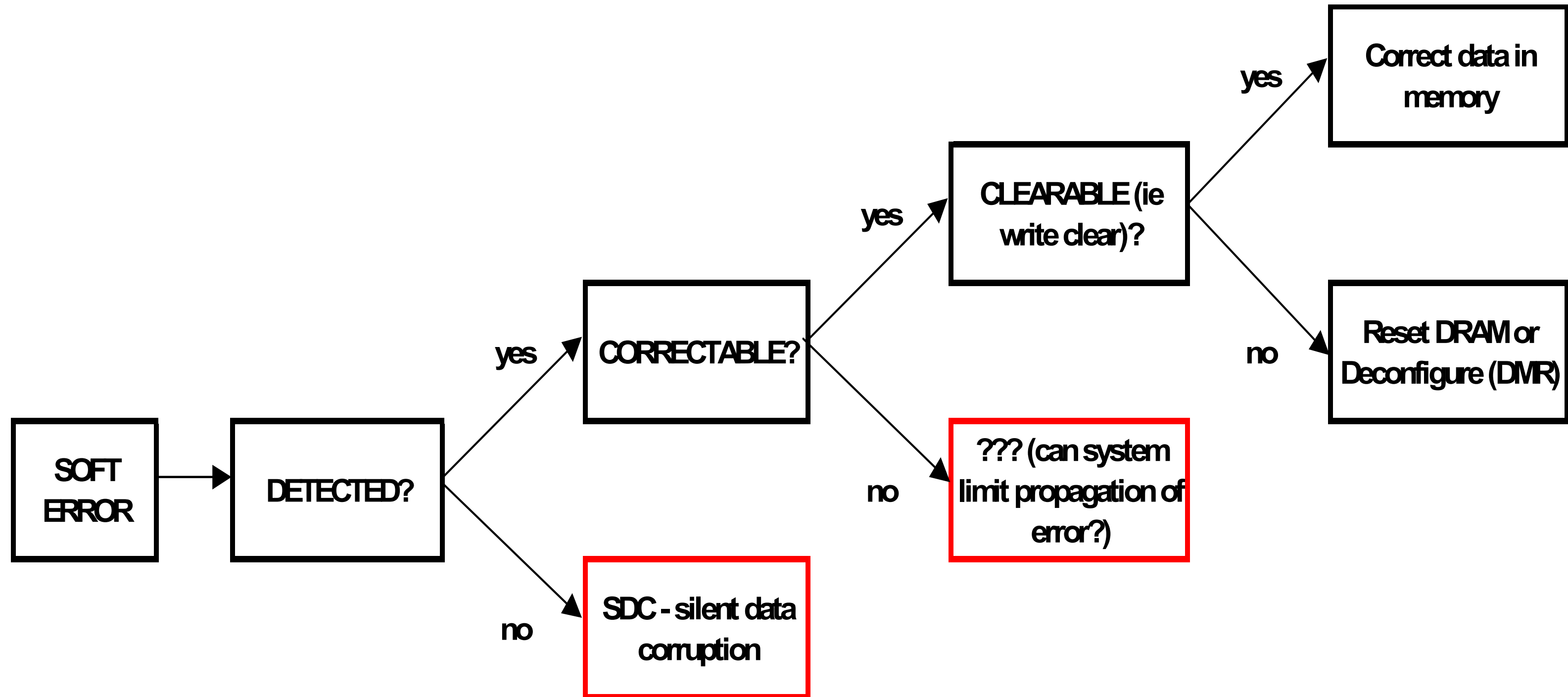
ECC Code	Single-Cell	Multi-Cell		kcell UPSET			
				Rewriteable		Power Cycle/Reset	
		Multiple Single-Bit	Multi-bit	Multiple Single-Bit	Multi-bit	Multiple Single-Bit	Multi-bit
SEC-DED (no interleave)	CE	CE	UE or SDC	CE	UE or SDC	CE (hard)	UE or SDC (hard)
SEC-DED (interleave)	CE	CE	CE	CE	CE	CE (hard)	CE (hard)
SBC-DBD	CE	CE	CE	CE	CE	CE (hard)	CE (hard)

- CE = correctable error, UE = detectable but not correctable, SDC = silent data corruption
- Hard = soft error not clearable by simple re-write. DRAM reset or power-cycle required.
- SEC-DED(interleave) and SBC-DBD codes are capable of "chipkill" or Single Device Data Correction (SDDC)

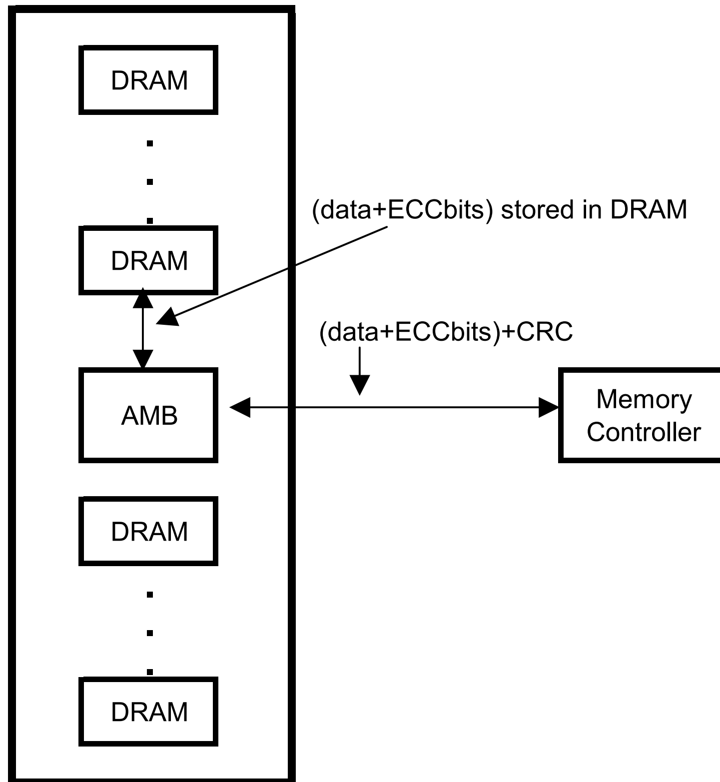
Dynamic Memory Reconfiguration

- Needed for logic soft errors that cannot be cleared by simple rewrite
- Various Implementations
  - Memory Mirroring – costly (2x memory required)
  - Memory Sparing – more cost effective, but spare memory is unused if no kcell events experienced
  - Bit Steering – kcell events don't always line up with single DQ pin
  - Memory Page Retire – analogous to bad sectors on hard drive, no added cost, good granularity (8KB), no impact on performance

DRAM Soft Error Mitigation



Future Issues – Fully Buffered DIMM



- Neutron Strikes in DRAM
  - Isolated to a single chip (either logic or cells)
  - Correctable with “chipkill” or SDDC codes
- Neutron Strikes in Advanced Memory Buffer (AMB)
  - Upset of (data+ECCbits) not from same DRAM → not correctable (ie no added ECC protection of AMB cache)
  - Upset of CRC circuits → will retry or reset fix it?

Conclusions

- Accelerated neutron beam testing required to probe details of DRAM soft errors
- Multi-cell → Multi-bit upsets do exist with some vendors
- Logic upsets manifest as kcell errors are not scaling will cell upsets
- "Chipkill" or SDDC codes will be required for high reliability server applications
- Neutron beam testing of AMB will be required to validate reliability of FB DIMM