

Assessing the Impact of Scaling on the Efficacy of Spatial Redundancy based SER Mitigation Schemes

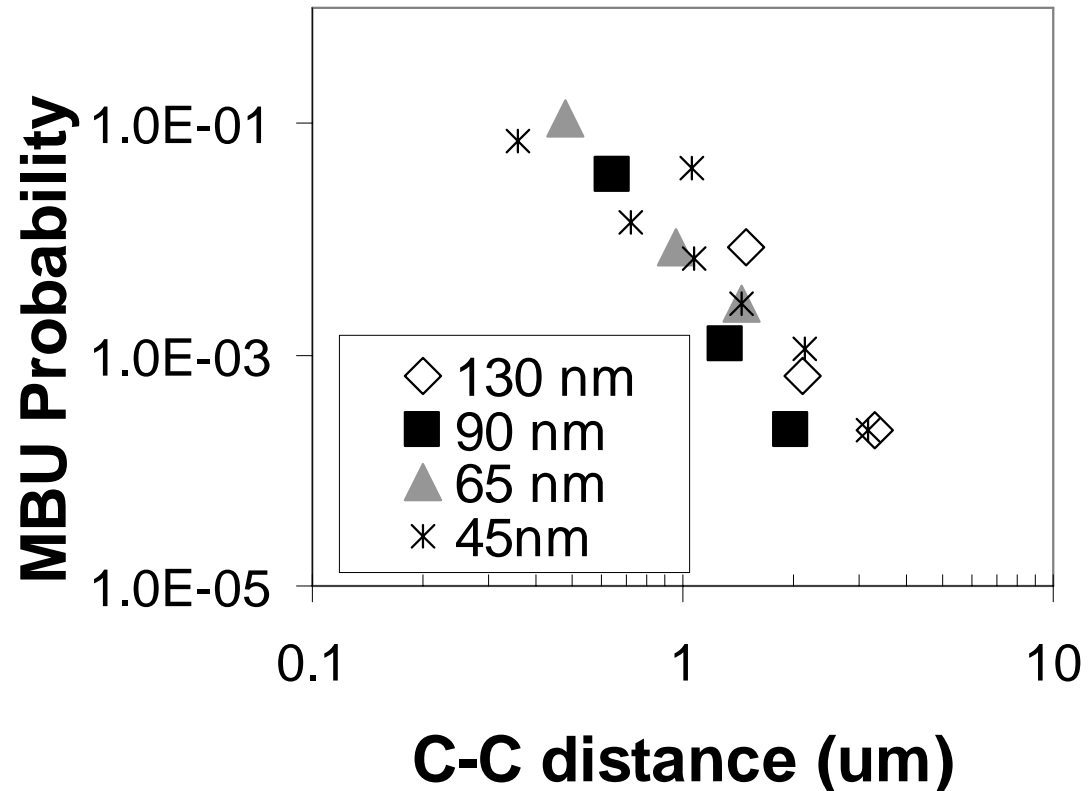
N. Seifert, B. Gill, V. Ambrose, M. Zhang, V. Zia

Intel Corporation, USA

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Motivation

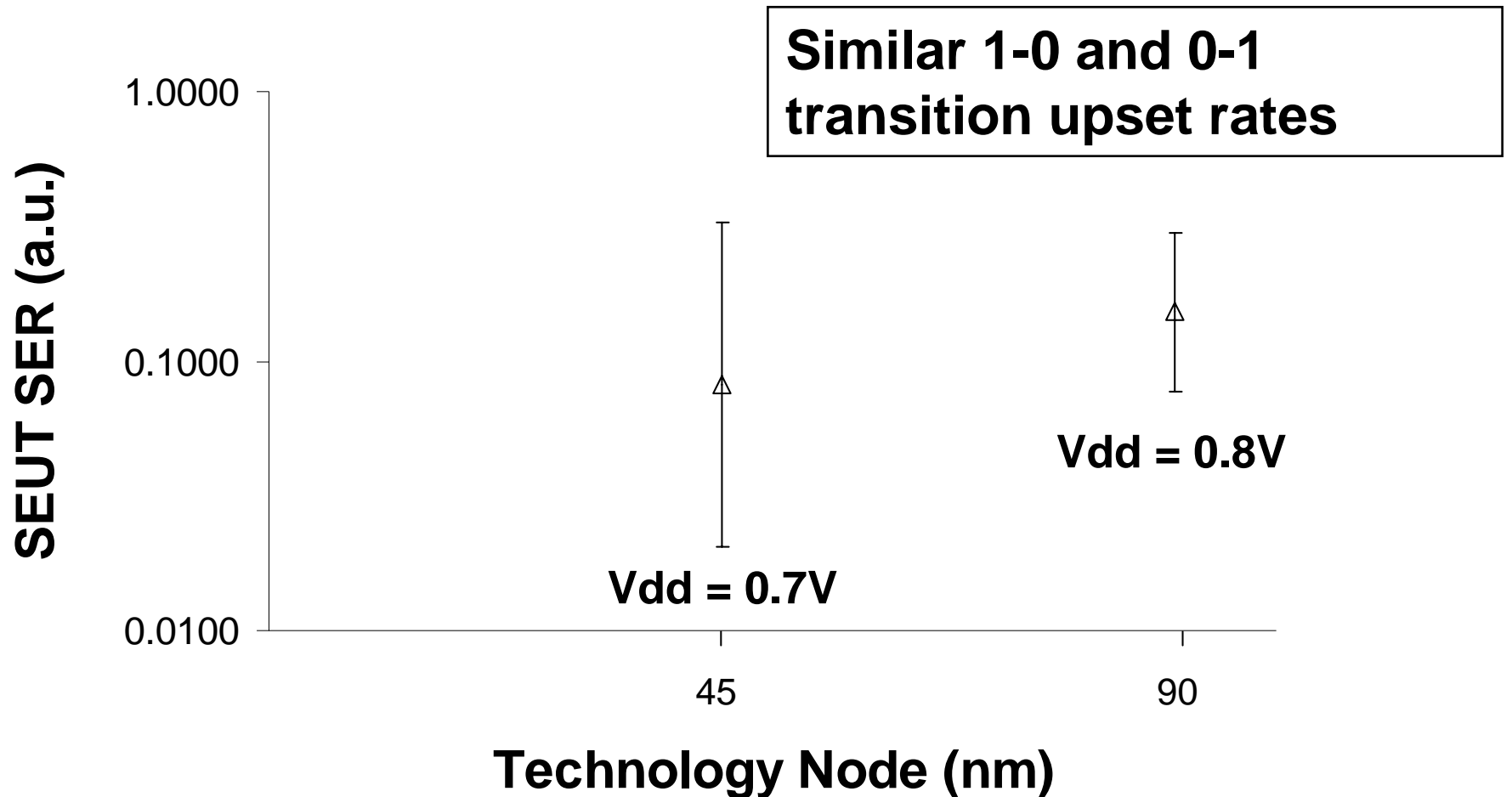
- **SRAM MBU SER Trend**
 - Increasing degree of charge sharing
 - Exponential increase in MBU rates with decreasing cell pitch
 - Consistent trend over several technologies



What is the impact of charge sharing on the SER of hardened circuits that utilize local redundancy?

Experimental Results

- Flat SEUT SER trend => **Redundancy hardened design scalable! Really?**



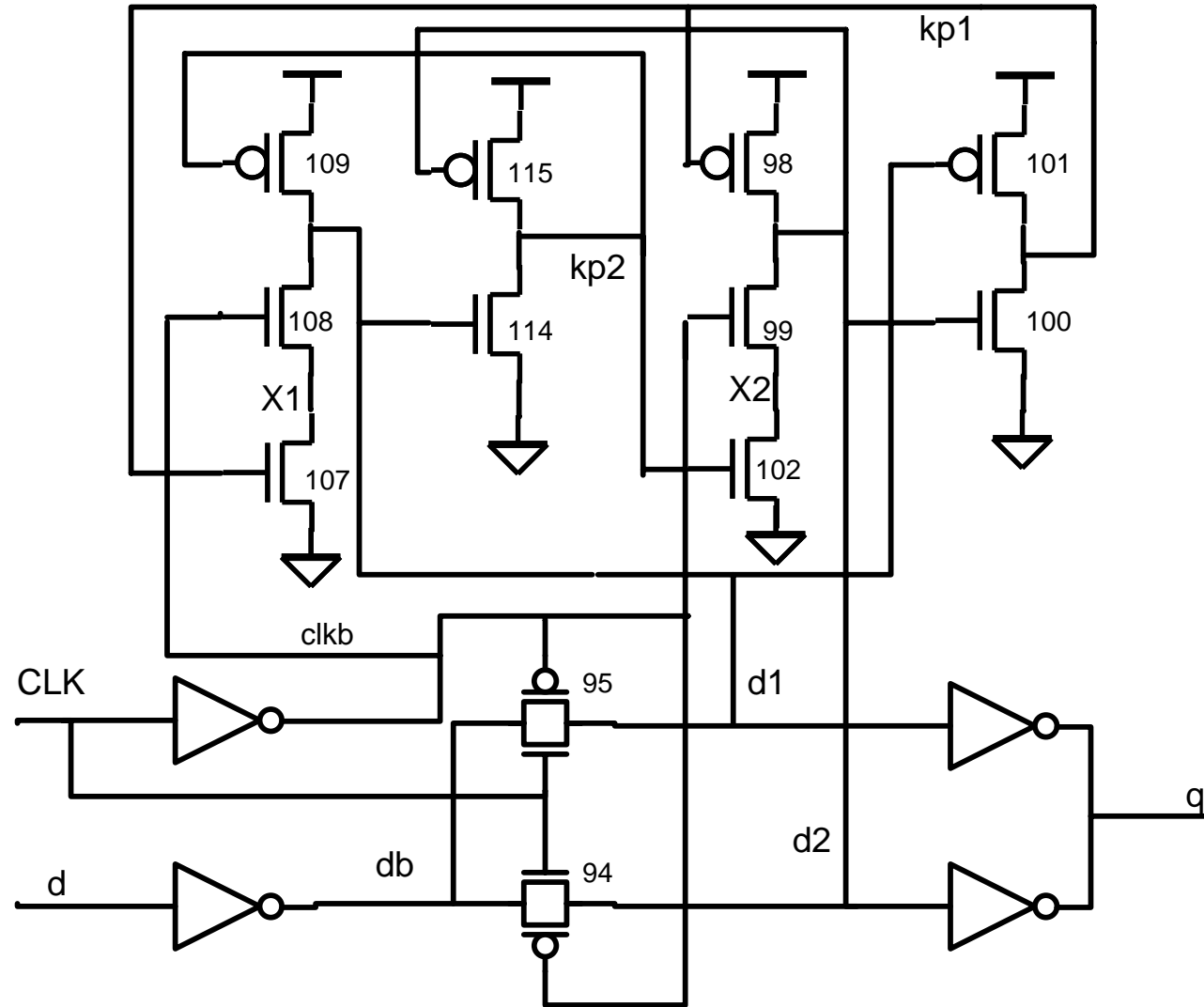
Outline

- **Introduction**
 - Investigated Hardened Devices
 - Experimental Setup
 - Charge Sharing Simulation Methodology
- **Charge Sharing Simulation Results**
 - SEUT
 - BISER
- **Technology Trend**
- **Conclusions**
- **Backup Material**

Investigated Hardened Devices

- **SEUT**

- Principle: Dual node feedback control (DICE)
- two redundant interlocked and interruptible keepers
- Split buffers to minimize glitches



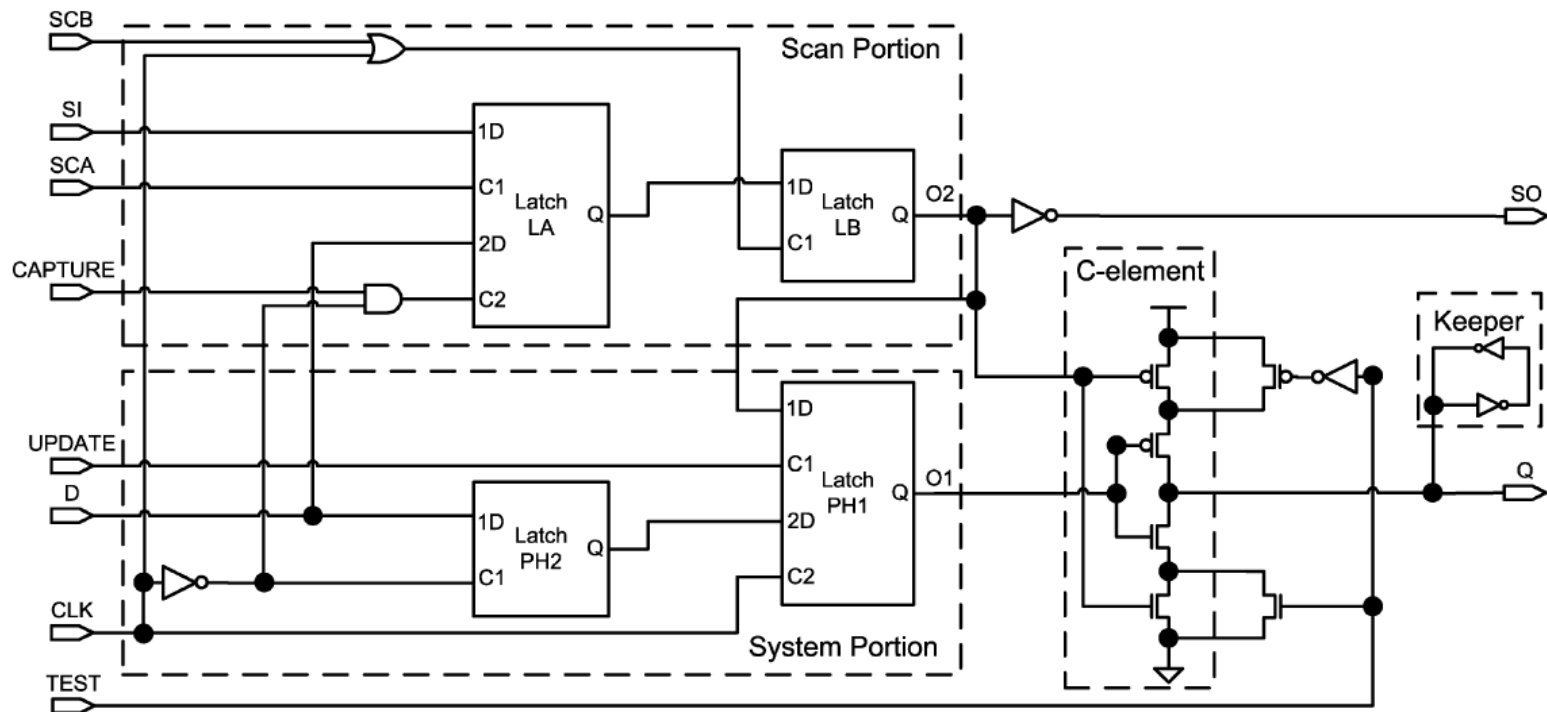
Upset Modes:

- a) Clock node strikes and b) ≥ 2 nodes upset simultaneously

Investigated Hardened Devices

- **BISER**

- Principle: Two latches/FFs joined with a C-element
- Error blocking; no glitch propagation

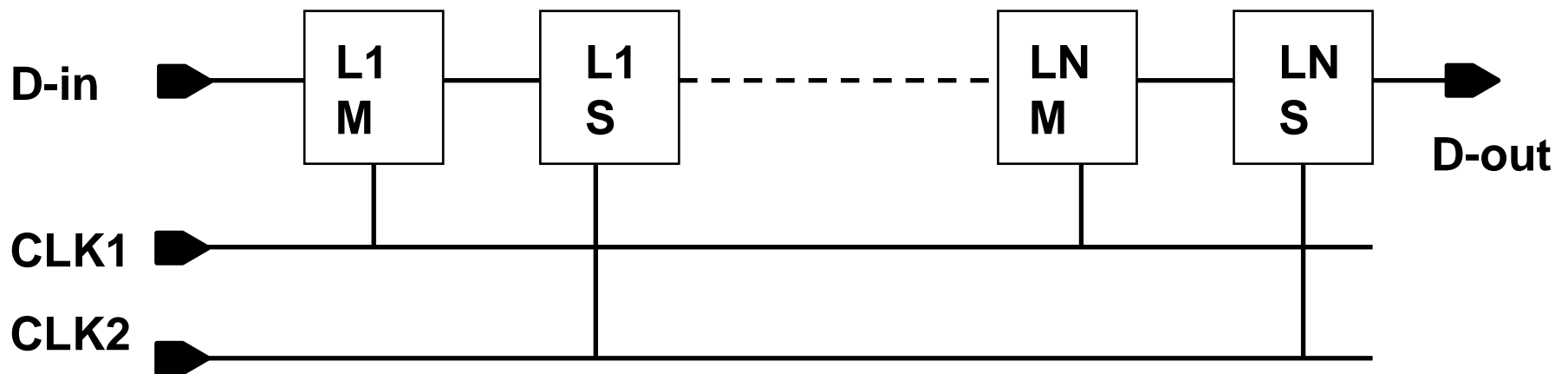


Upset Modes:

a) Clock node strikes and b) ≥ 2 nodes upset simultaneously

Experimental Setup

- **Test-chip: Shift register architecture**
 - Built in 45nm metal gate process
 - 90nm data + schematics made available by T. Karnik and P. Hazucha



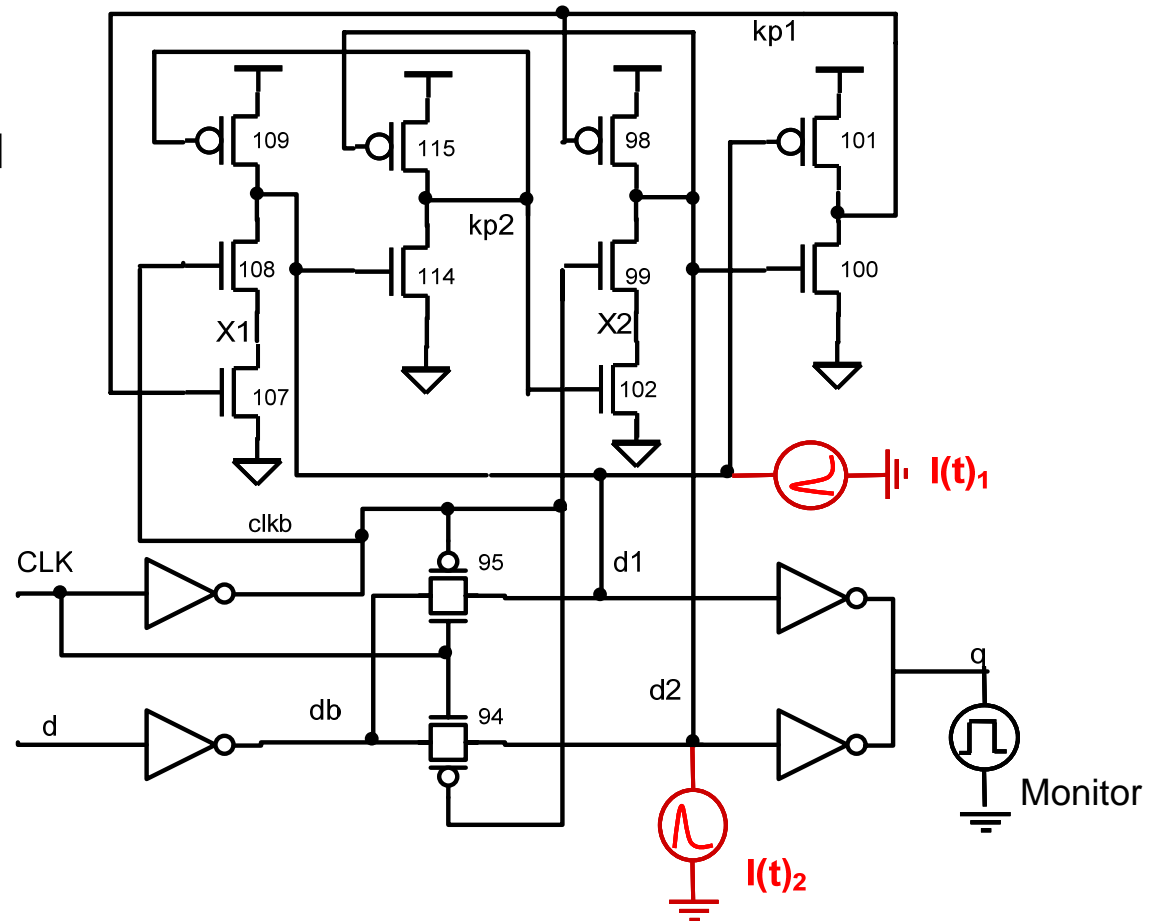
- **Measurements: Weapons Neutrons Research (WNR) facility, Los Alamos, New Mexico**

Charge Sharing Simulation Methodology

- **Physical Device Simulations**
 - **3D Mixed Mode: Most accurate**
 - **Currently not feasible**
 - ~72 hours per particle strike for small cell
 - Monte Carlo methodology requires 100s if not 1000s of strikes to be simulated
- **Circuit-level**
 - **Qcrit based scheme**
 - Two or more charge collection current waveforms
 - **Idea: Apply SBU circuit-level methodology to simulation of strikes involving >1 nodes**
 - SBU: SER is function of Qcrit and charge collection area A
 - **Method of choice in this work**

Charge Sharing Simulation Methodology

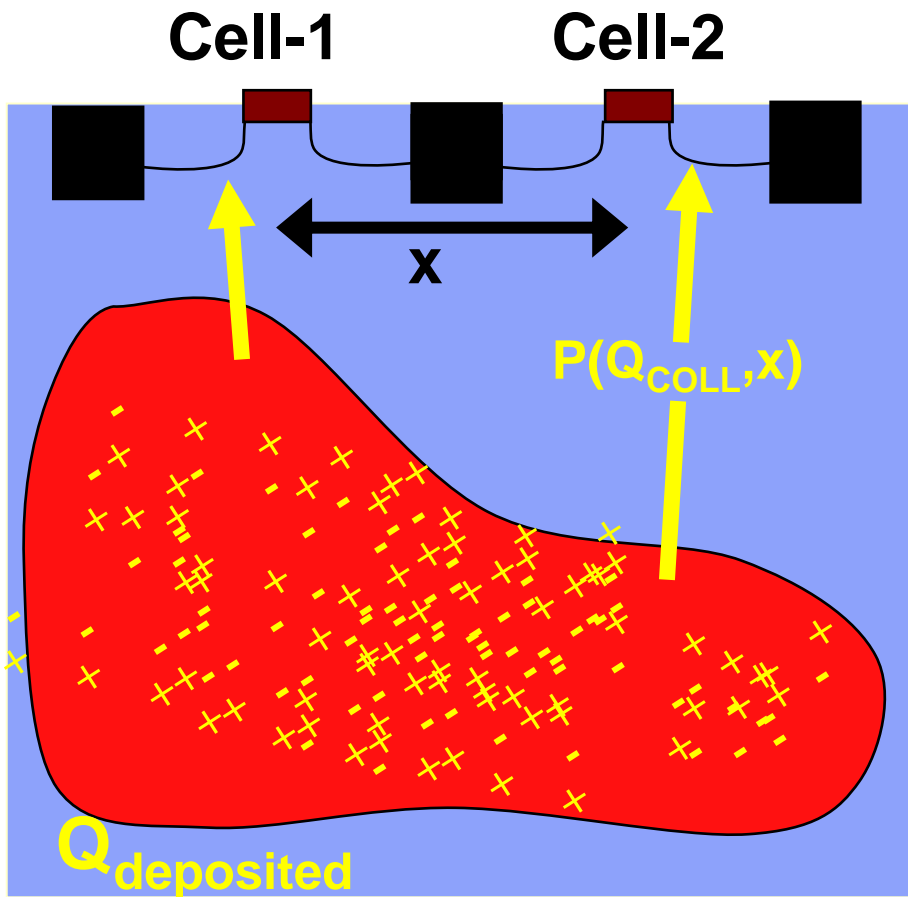
- Inject current at **2 nodes** simultaneously
 - Primary and secondary coupled nodes
 - All combinations
- Determine Q_{crit}
 - Q_{crit} defined by charge collected at primary node
 - Fixed $R = \text{ratio of } I_{peaks}$
 - $Q_{crit}(R) \Rightarrow Q_{crit}(Q_s)$
- SER function of Q_{crit} and A
 - Same function as for SBU
- Integrate SER over probability $P(Q_s, x, A)$ to collect charge Q_s at secondary node
 - Every node is once primary and secondary node \Rightarrow factor 1/2



$$SER^{CS} = \frac{1}{2} \sum_{\text{node-j}} \frac{\left(\sum_{Q_s} P(Q_s, x, A) * SER(Q_{crit}^j(Q_s(x), A_j)) \right)}{\sum_{Q_s; x'} P(Q_s, x', A)}$$

Charge Sharing Simulation Methodology

$$\text{prob}_{\text{MBU}}(Q_{\text{CRIT}}, X) = \frac{N_k^{\text{upsets}}}{N_1^{\text{upsets}}}$$



x denotes the size of the MBU cluster

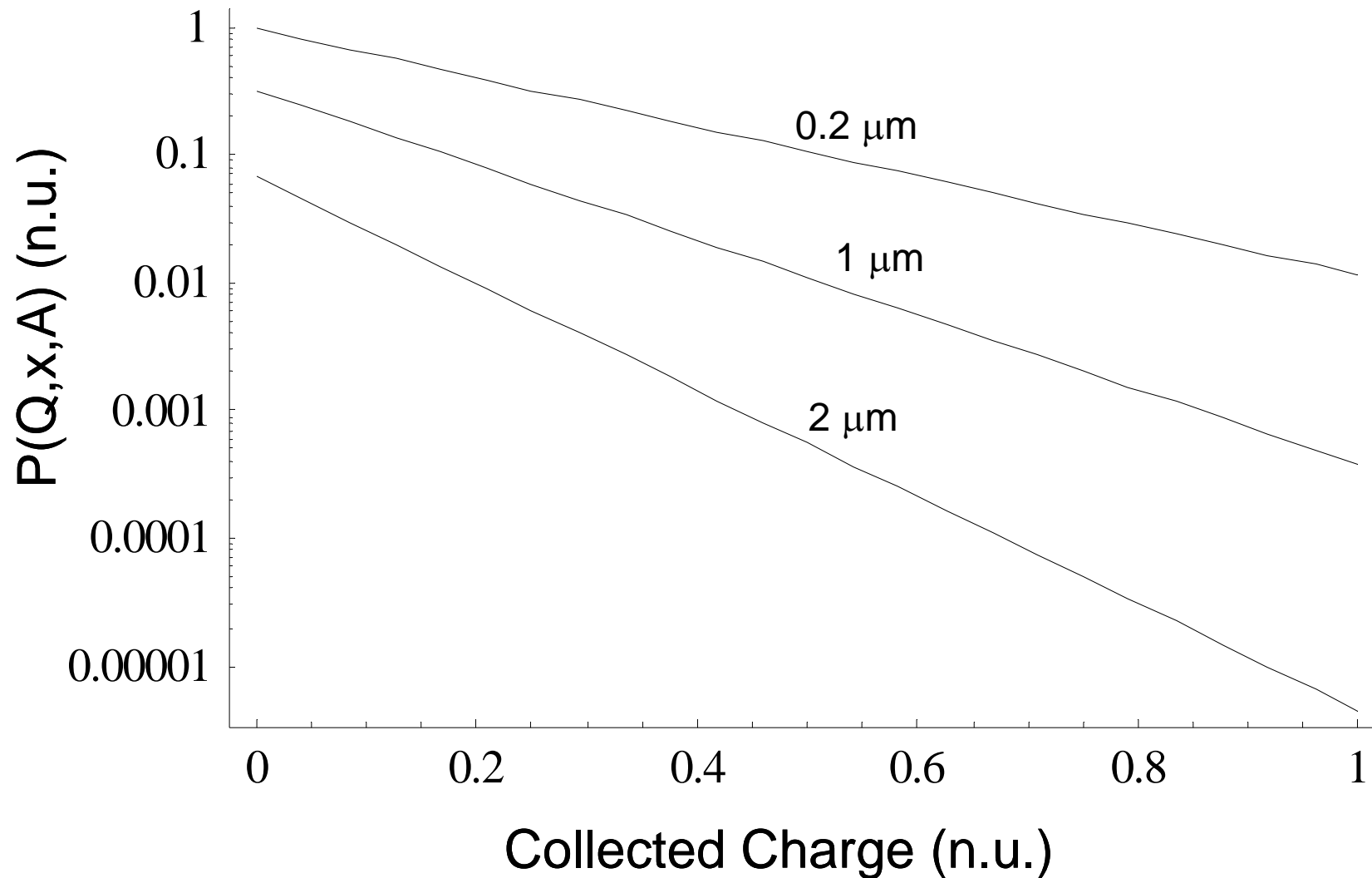
$P(Q, x, A)$ = probability to collect charge Q at distance x .

By varying $V_{\text{dd}} (\propto Q_{\text{CRIT}})$ and investigating SRAM-MBU cluster stats of different cluster sizes one can extract $P(Q, x, A)$

$$\text{prob}_{\text{MBU}} \approx \frac{Q_{\text{CRIT}} \int_{Q_{\text{CRIT}}}^{\infty} P(Q_{\text{COLL}}, x) dQ_{\text{COLL}}}{\int_{Q_{\text{CRIT}}}^{\infty} P(Q_{\text{COLL}}, 0) dQ_{\text{COLL}}}$$

$P(Q, x, A)$ average over N-N and P-P strikes. N-P and P-N strikes neglected.

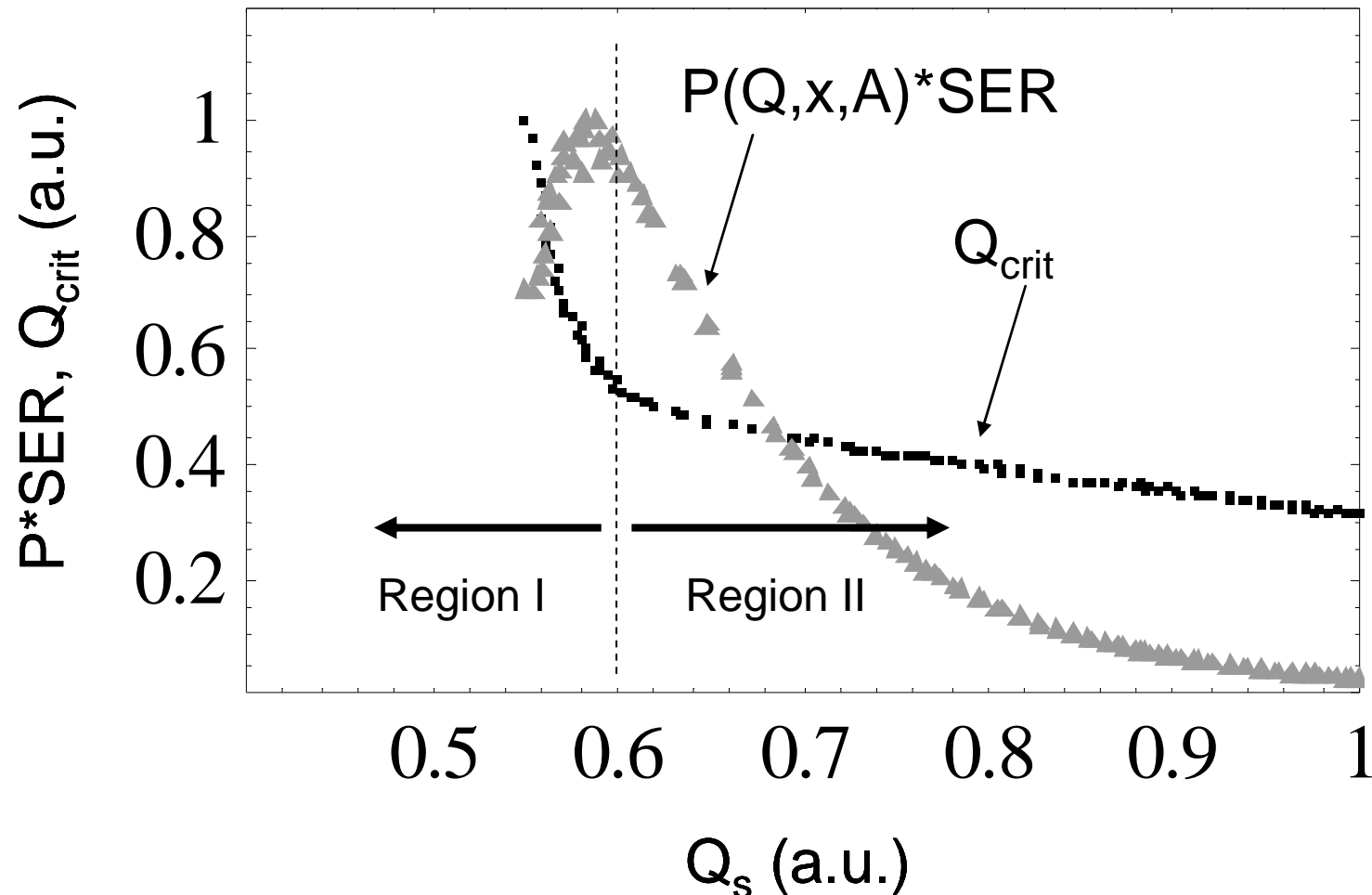
Charge Sharing Simulation Methodology



$P(Q, x, A)$ decreases steeply with Q_{coll} and node separation

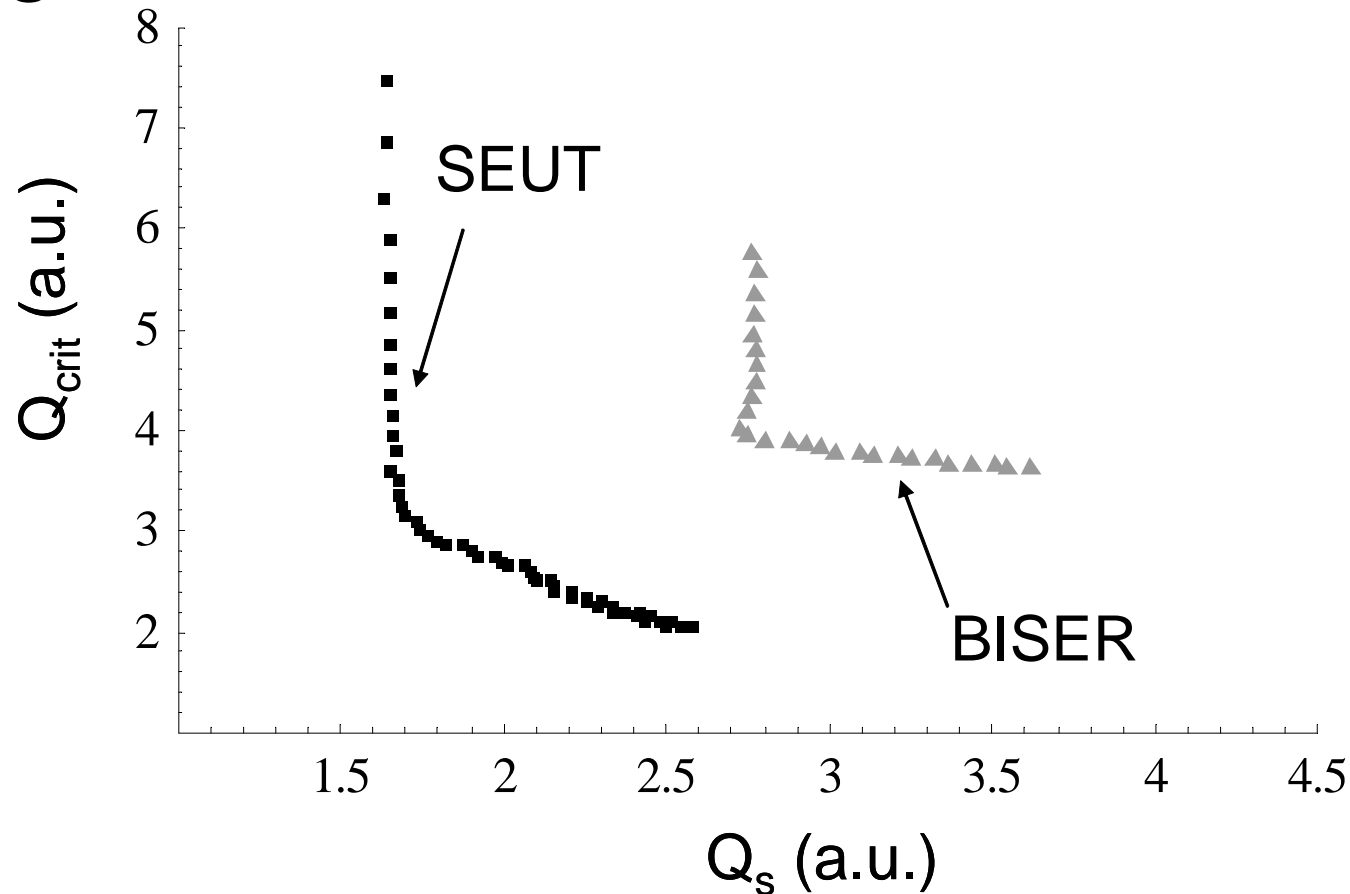
Simulation Results

- Q_s threshold: region I
- If more charge Q_s is collected at secondary node => Q_{crit} of primary node decreases (SEUT): region II



Simulation Results

- BISER shows more pronounced threshold
- Higher critical charges (less coupling/feedback)
- Larger cell => more freedom to separate critical nodes

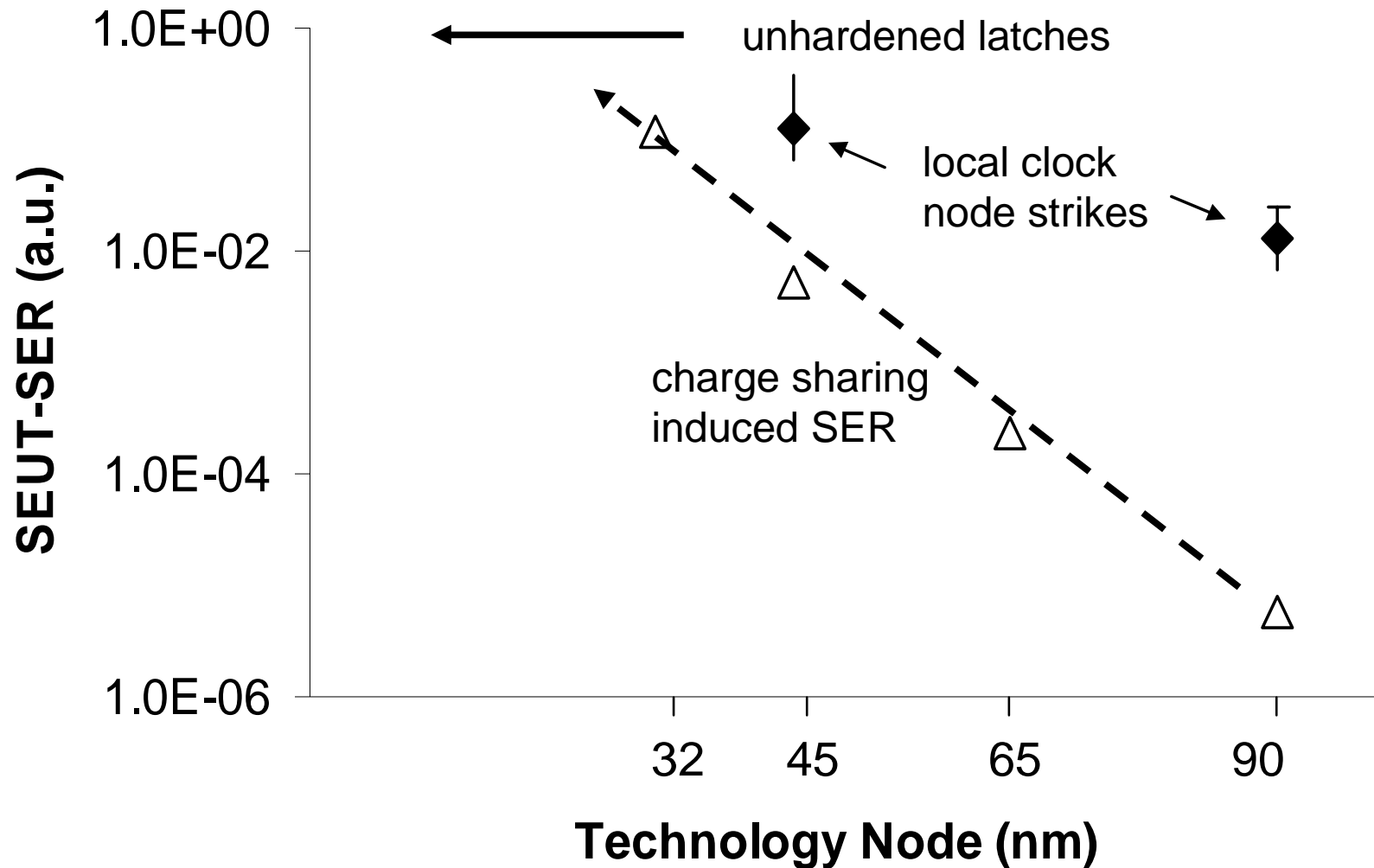


Simulation Results

- **Measured SER data reflect clock node strikes and not charge sharing**
 - **Experimental data consistent with clock node strike simulation results**
 - **1-0 and 0-1 asymmetry (due to layout topology) and absolute SER not reflected in experimental data**

Device	Technology (nm)	Vcc (V)	Nodes	min Distance (n.u.)	SER (n.u.)
SEUT-meas	45	0.7	NA	1	0.0818
SEUT-meas	90	0.8	NA	5	0.1518
SEUT	45	0.7	1->0 only	1	0.0257
SEUT	45	0.7	0->1 only	2.5	0.0007
SEUT	45	0.7	all	1	0.0132
SEUT	45	0.7	clkb	NA	0.1051
SEUT	90	0.8	all	5	3.97E-08
SEUT	90	0.7	all	1	0.0350
SEUT	90	0.8	clk node	NA	0.0934
BISER	45	0.7	all	3	1.17E-08
BISER	45	0.7	all	1	1.17E-05

Technology Trend



Voltage scaling and node separation scaling might render this type of hardening ineffective in only a few generations

Conclusions

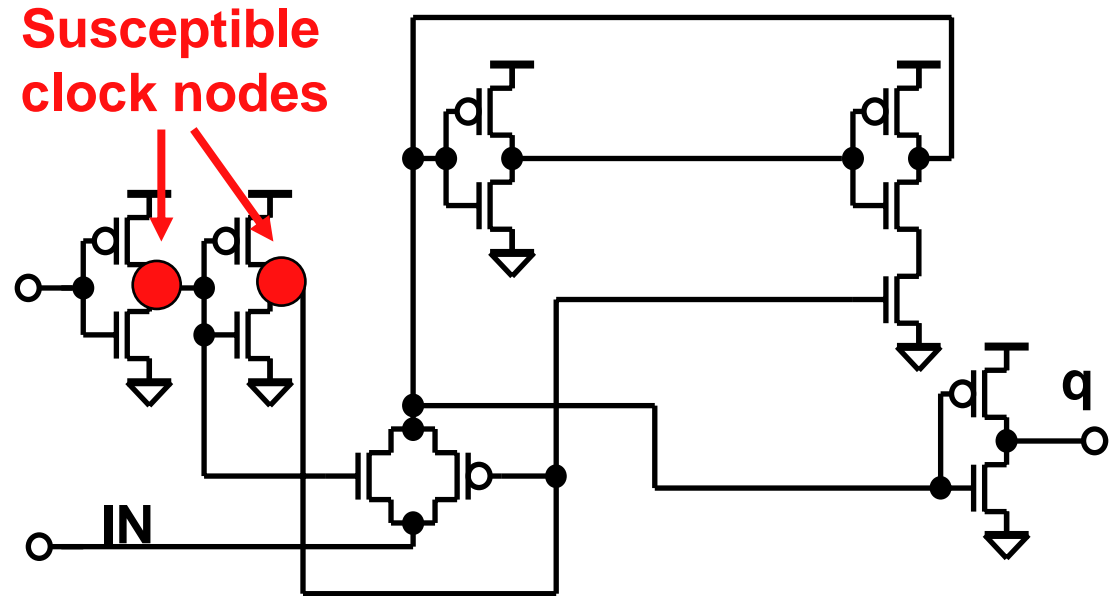
- **Introduced novel circuit-level strategy to simulate impact of charge sharing on SER of hardened latches**
 - **Compared to measured 90nm and 45nm SEUT SER data**
- **Results provide strong evidence that error rates of investigated hardened latches are dominated by clock node upsets and not charge sharing**
- **Projected SER trend indicates that within 2-3 process generations hardening utilizing local redundancy might become ineffective**
 - **Due to the impact of charge sharing**
 - **Without any “intelligent” layout optimization**
 - **BISER projected to perform better than SEUT/DICE**

Backup Material

Hardened Cells Upset Modes

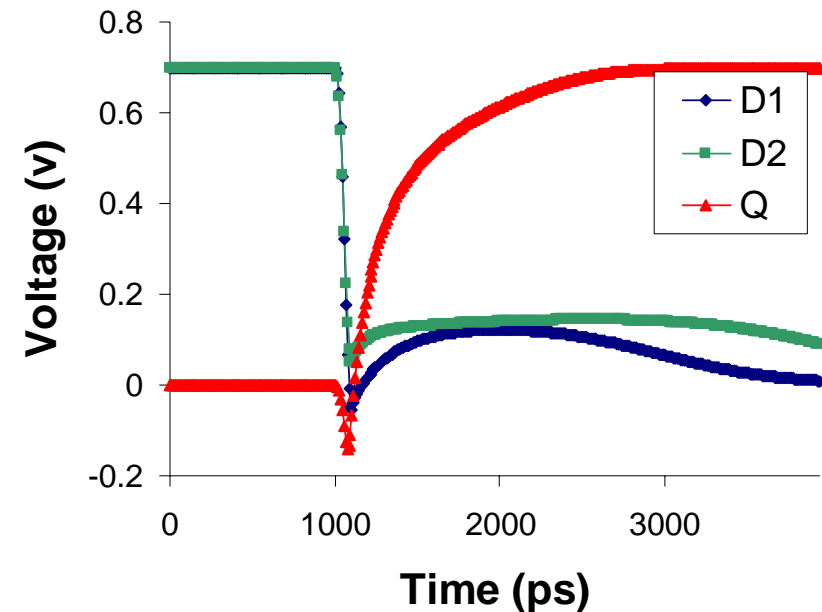
- **Local Clock Node Strikes**

- “Radiation-induced Race”
- Transmission gate temporarily open
- Data corrupted if different data at IN

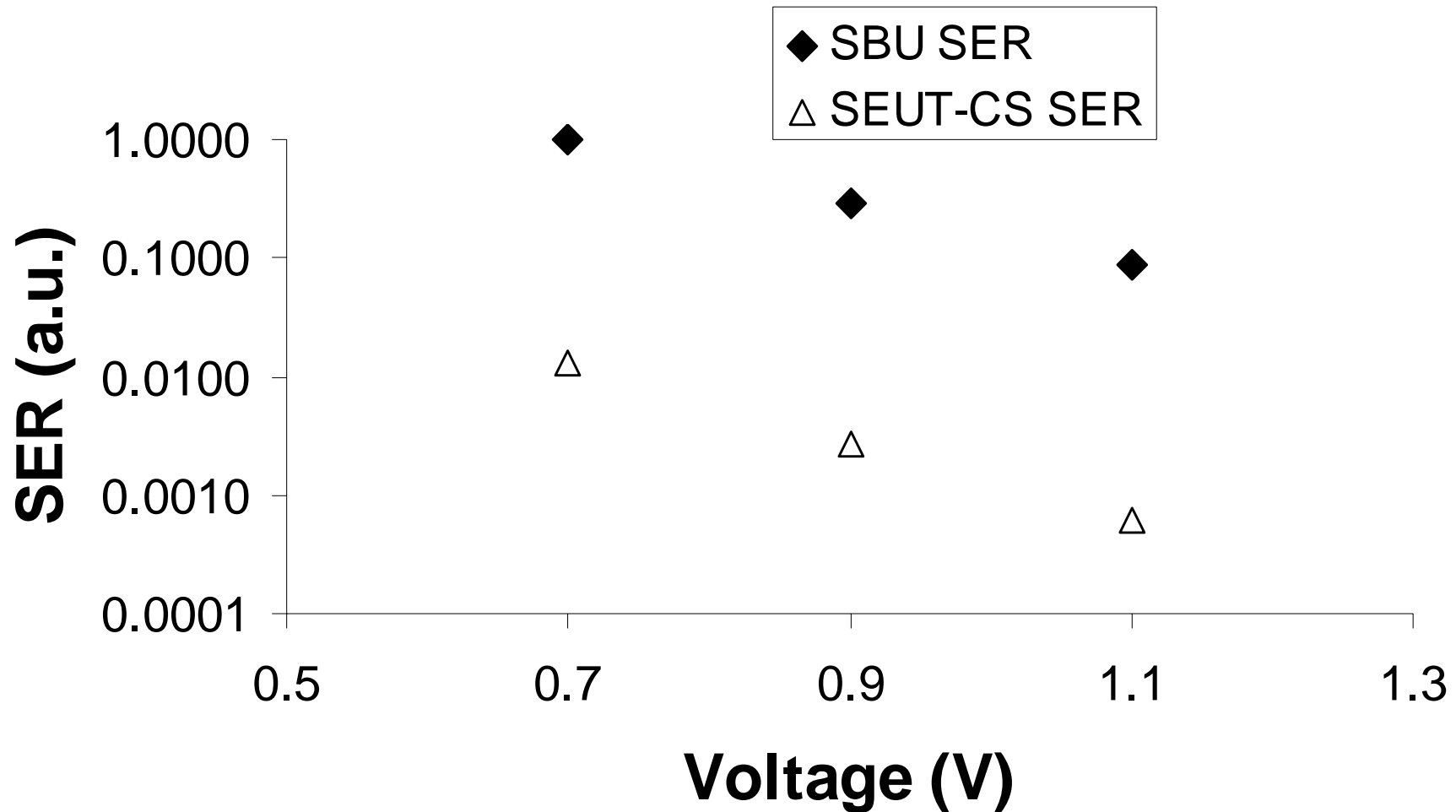


- **Charge Sharing**

- 2 or more redundant nodes (d1 and d2 in example to the right) collect charge generated by one particle strike

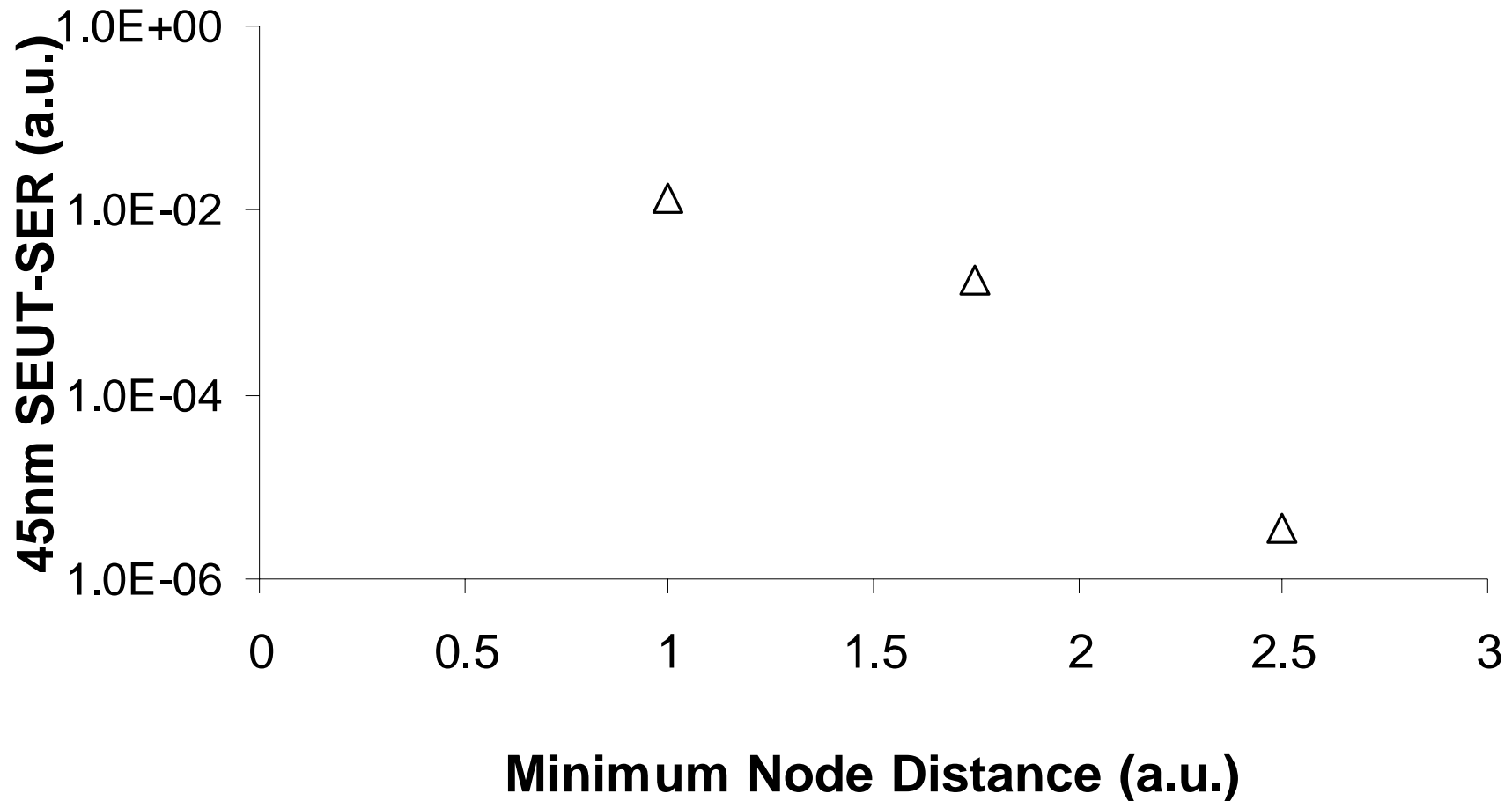


Voltage Trend



Slope larger in the case of charge sharing

Node Separation Trend



Steep decrease with increasing node separation