



Call for Participation
SELSE-3 Workshop
Silicon Errors in Logic - System Effects
April 3rd & 4th, 2007
Austin, Texas

The growing complexity and shrinking geometries of modern device technologies are making these high-density, low-voltage devices increasingly susceptible to influences from electrical noise, process variation, and natural radiation interference. System-level effects of these errors can be far reaching. Growing concern about intermittent errors, erratic storage cells, and the effects of aging are influencing system design. This workshop provides a forum for discussing current research and practices in system-level error management. Participants from industry and academia explore both current technologies and future research direction (including nanotechnology). We are interested in soliciting papers that cover system-level effects of errors from a variety of perspectives: architectural, logical and circuit-level, and semiconductor processes. Case studies are also solicited.

Key areas of interest are (but not limited to):

- Technology trends and the impact on error rates.
- New error mitigation techniques.
- Characterizing the overhead and design complexity of error mitigation techniques.
- Case studies describing the engineering tradeoffs necessary to decide what mitigation technique to apply.
- Experimental data.
- System-level models: derating factors and validation of error models.
- Error handling protocols (higher-level protocols for robust system design).

Authors are requested to submit their extended abstracts for review **before December 20, 2006**. Guidelines for submission are available at www.selse.org. Submissions should be PDF or Microsoft Word files that do not exceed four printed pages. Customary terms for copyright agreement and non-confidentiality will apply. Authors will be notified of paper outcome by March 2, 2007. The camera-ready formatted papers are due on March 23, 2007.

Registration information is posted on the workshop website: www.selse.org

Organizing committee:

Workshop Co-chairs Wendy Bartlett (HP) Pia Sanda (IBM)	Program Co-chairs Dennis Abts (Cray) Subhasish Mitra (Stanford)	Web Chair Jeff Wilkinson (Medtronic)
Publications Chair Norbert Seifert (Intel)	Publicity Co-Chairs Cristian Constantinescu (Intel) Babak Falsafi (CMU)	Local Arrangements Chair Nur Touba (UT Austin)
Finance Co-chairs Nhon Quach (AMD) Vivian Zhu (Texas Instr)	Panel Co-Chairs Ishwar Parulkar (Sun) Josep Torrellas (Univ Illinois)	Advisory Committee Sarita Adve (Univ Illinois) Ravi Iyer (Univ Illinois) Chuck Moore (AMD) Lisa Spainhower (IBM)